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10Gb/s transmit equalizer using duobinary signaling over FR4 backplane①

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Abstract

A 10Gb/s 6-tap transmit equalizer based on partial response signaling for high speed backplane transmission is presented. By combining features of equalizer and frequency-dependent channel, duobinary signaling can be generated at the output of FR4 backplane, aiming at increasing data rate while reducing design complexity. Based on 0.18μm CMOS technology, this equalizer has been designed and fabricated, in which both variable capacitor and load resistor calibration techniques are explored to eliminate the effect of process variations. The chip occupies $0.68 \times 0.8 mm^2$ including I/O pads and consumes a power of 194mW with 1.8V power supply. Measurement results show that a typical 3-level eye diagram can be obtained at the receiver and the equalizer can work properly at the data rate of 10Gb/s.

Key words: transmit equalizer, duobinary, partial response, load resistor calibration, CMOS technology

0 Introduction

The demand for high performance data communication over backplane and chip-to-module has been increasing dramatically. When data rate increases, received data will be seriously damaged and the signal integrity will be severely impaired due to dielectric loss proportional to the frequency and skin effect which is proportional to the square root of the frequency. To enhance signal integrity, the most commonly used equalization techniques for high-speed backplane include decision feedback equalization (DFE) and feed-forward equalization (FFE), either in receiver or in transmitter. DFE is a nonlinear equalization technique and has some drawbacks such as error propagation. Apart from it, DFE can only compensate postcursor inter symbol interference (ISI) while FFE can compensate both postcursor and precursor. As a linear equalizer, FFE is normally designed as a FIR filter and can be used in high speed serial link due to its simplicity and good performance[1-3].

With the rapid increase of data rate, however, traditional non-return-zero (NRZ) based equalizer faces more and more challenges due to the limitation of process. To alleviate the problem, alternative modulations such as PAM4 and duobinary are adopted to reduce the bandwidth requirement effectively. It has been known that a 3-level modulation duobinary can reduce the bandwidth requirement to half of that for NRZ and has a bandwidth requirement on par with PAM4 which is a 4-level modulation scheme. It is obvious that duobinary and PAM4 modulation outperform NRZ in bandwidth requirement of transceiver.

Because of its 4 levels, however, the receive system for PAM4 is more complex compared to that of duobinary signal. In addition, for the same average signal power and channel noise, the signal integrity of PAM4 is far more vulnerable to deterioration when compared with that of duobinary[4].

Motivated by increasing data rate while reducing design complexity, this work explores a transmit equalizer based on partial response signal, i.e. duobinary signaling. Different from typical equalizer which compensates the loss of channel as much as possible, this equalizer just needs to compensate channel loss partially and make the output of channel be a duobinary signal. More importantly, the feature of band-limited channel can be used in generating duobinary signals.

1 Architecture design

From the view of timing, duobinary signaling

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firstly proposed by Lender allows controlled amount of inter symbol interference and can be expressed as the sum of current bit and the former one as following:

$$y(n) = x(n) + x(n-1) \quad (1)$$

where, $y(n)$ and $x(n)$ are the output and input at time n, respectively, and $x(n-1)$ is the input at time $n-1$. It indicates that a duobinary signal can be generated with ease by adding adjacent pulse responses whose spacing is one symbol[5].

The working principle of the equalizer will be analyzed first from the view of frequency domain. See Fig. 1, a typical frequency-dependent channel has a roll-off that is much steeper than that of desired duobinary signal. As a result, the proposed equalizer which is in fact an equalization filter should have appropriate high-frequency boost to generate a duobinary signal at the end of channel. However, the amount of high-frequency boost is significantly reduced when compared to NRZ signaling since the duobinary frequency spectrum has a null at half the bit rate, providing a distinct advantage. In other words, by the combination of the channel response and the FIR filter, required duobinary response can be realized[6].

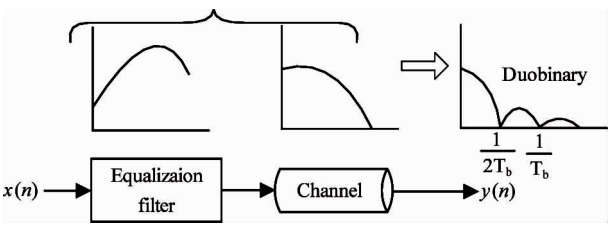

Fig. 1 Working principle of the proposed equalizer

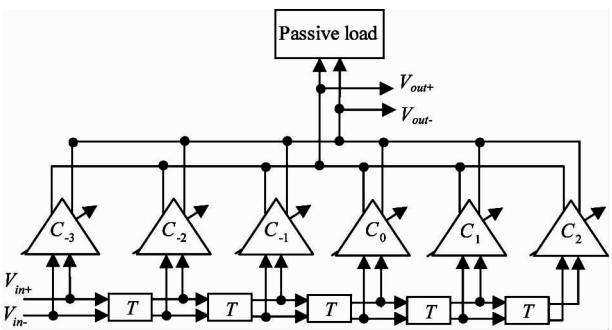

Fig. 2 Block diagram of the proposed filter

To realize the equalization filter with high frequency boost, a 6-tap FIR filter with 5 delay units is designed in this paper, shown as Fig. 2. Its output can be expressed as

$$V_{out} = \sum_{i=-3}^{2} C_i \cdot V_{in}((n-i-3)T) \quad (2)$$

where V_{in} is the input, $C_i(i=-3,-2,\cdots,2)$ is the i^{th} tap coefficient, and T is the period of one symbol.

From Fig. 2, it can be seen that the input and its delay signals are multiplied by C_i first and then summed together. After that, the summed current is converted to the output voltage V_{out} by the load resistors. It is obvious that a desired performance of the filter can be acquired by optimizing the delay unit and the value of tap coefficients[7].

2 Circuit design

2.1 Delay unit

The delay line plays an important role in the filter and can be realized as a passive pattern or an active one. In our design an active structure is employed since it is invulnerable to process variation and occupies less area when compared to a passive one. The active delay line, however, is difficult to meet the bandwidth requirements for 10Gb/s data rate especially in 0.18μm CMOS technology. Consequently, a structure with source degeneration capacitance is employed to expand the bandwidth. See Fig. 3, the transfer function of the delay unit can be given as

$$A_V(S) = \frac{G_{m3}R_L(1+SR_SC_S/2)}{(1+SC_LR_L)(1+G_{m3}R_S/2+SR_SC_S/2)} \quad (3)$$

where G_{m3} is the transconductance of M3, C_L is the load capacitance and C_S is the source degeneration capacitance. It can be observed that there are two poles: $p_1=(G_mR_S+2)R_SC_S$, $p_2=1/C_LR_L$ and one zero $z_1=2/(R_SC_S)$. If z_1 is placed in front of p_1 and p_2, the circuit will be peaked and the purpose of expanding the bandwidth can be realized. Practically, the position of the zero is adjusted by changing the bias voltage of variable capacitor C_S[8,9].

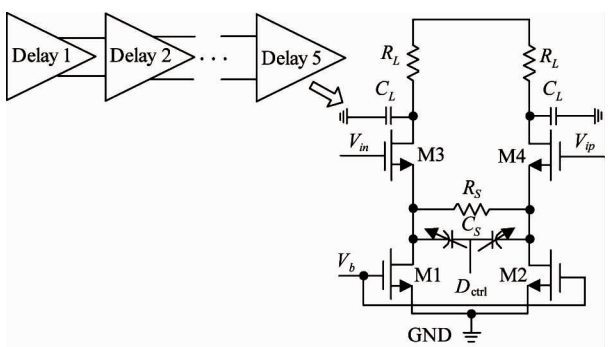

Fig. 3 Delay unit with source capacitive degeneration

2.2 Delay line optimization using calibration techniques

As mentioned above, the accuracy of delay line is important to the performance of filter. Below the delay circuit from the view of group delay will be analyzed

and optimized. The group delay of the proposed delay unit can be expressed as

$$GroupDelay(w) = -\frac{\partial\varphi}{\partial w} = -\frac{1}{1+\left(\frac{w}{z_1}\right)^2}\cdot\frac{1}{z_1}+\frac{1}{1+\left(\frac{w}{p_1}\right)^2}\cdot\frac{1}{p_1}+\frac{1}{1+\left(\frac{w}{p_2}\right)^2}\cdot\frac{1}{p_2} \quad (4)$$

When frequency is low ($w \ll z_1$), Eq. (4) can be simplified as

$$GroupDelay(0) = -\frac{1}{z_1}+\frac{1}{p_1}+\frac{1}{p_2} = R_L C_L - \frac{G_{m3}R_S^2}{G_{m3}R_S+2}\times\frac{C_S}{2} \quad (5)$$

It can be inferred from Eq. (5) that the group delay is closely related to the zero. When C_S becomes large, the group delay is small, and vice versa. Thus, changing the capacitance of C_S by D_{ctrl}, the location of z_1 can be adjusted and the desired delay time can be obtained.

This can be illustrated further in Fig. 4, which gives the group delay versus D_{ctrl}. It can be viewed that the group delay is more sensitive to D_{ctrl} at low frequency. When the frequency goes high, however, the method of variable capacitor calibration is not effective, even worsens the flatness of group delay and leads to non-uniformity of bandwidth. This is because in this case both pole and zero will change with the process corner. Thus, making variable the two resistors R_L and R_S which determine the poles will allow improving the flatness of group delay at high frequency. This technique is also known as resistor calibration.

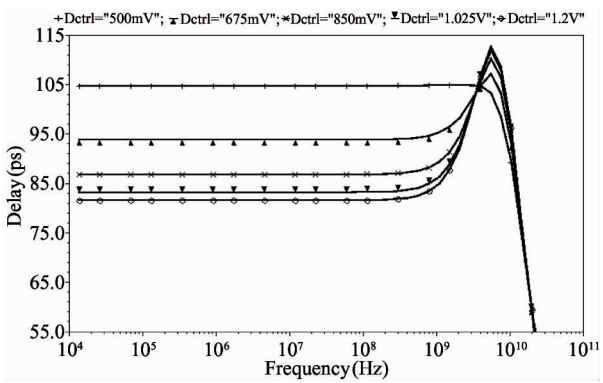

Fig. 4 Group delay of the delay line

Fig. 5 indicates the approach of resistor calibration in detail, in which load resistor R_L is replaced by shunt branches of resistors in series with PMOS switches $S_1 \sim S_3$. Meanwhile, source resistance R_S is also replaced by shunt branches of resistors in series with NMOS switches $T_1 \sim T_3$ which are logic reverse of $S_1 \sim S_3$. Using this resistor calibration technique, delay variations due to PVT (process, voltage, temperature) can be reduced effectively. It is worth noting that the resistance of each branch should be less than 15% of the total resistance in order to acquire high calibration accuracy and linearity.

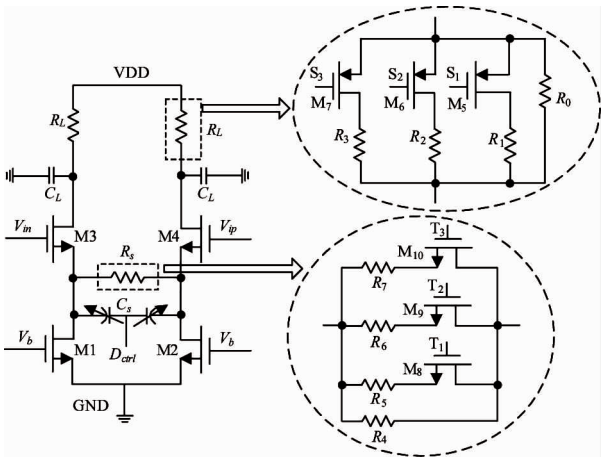

Fig. 5 Delay unit with resistor calibration

Fig. 6 shows the simulation result of delay time of the delay unit under different process corners. It can be observed that the flatness of the delay time is improved greatly by using capacitor and resistor calibration technique.

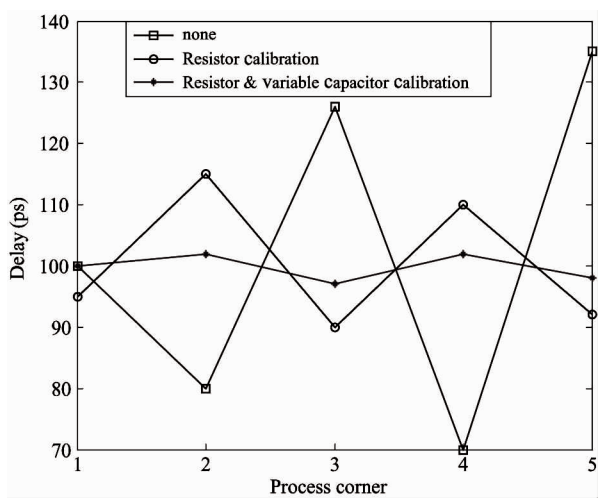

Fig. 6 Delay time under different process corners

2.3 Multiplier-summer

In this study, a multiplier-summer is designed based on current mode logic (CML), shown as Fig. 7. It can be seen that the input signal V_{in} and its delay versions are summed first in the form of current and then converted to the output voltage V_{out} through load resistance R_L.

The output voltage can be expressed as

$$\begin{aligned} V_{out} &= [\,G_{m-3}V_{in}(t+3T) + G_{m-2}V_{in}(t+2T) \\ &\quad + G_{m-1}V_{in}(t+T) + G_{m}V_{in}(t) \\ &\quad + G_{m+1}V_{in}(t-T) + G_{m+2}V_{in}(t-2T)\,]R_L \\ &= [\,C_{-3} + C_{-2} + C_{-1} + C_0 + C_1 + C_2\,]I_{SS}R_L \end{aligned} \tag{6}$$

where $G_{mi}(i=-3,-2,\cdots,2)$ are the input transconductances, $C_i(i=-3,-2,\cdots,2)$ are the tap coefficients and $C_0 I_{SS}$ is the current of the main tap.

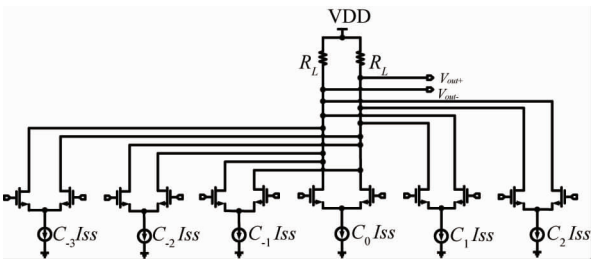

Fig. 7 CML based multiplier & summer

To obtain the optimal C_i, zero-forcing algorithm is used as

$$\begin{bmatrix} x_0 & x_{-1} & x_{-2} & x_{-3} & x_{-4} & x_{-5} \\ x_1 & x_0 & x_{-1} & x_{-2} & x_{-3} & x_{-4} \\ x_2 & x_1 & x_0 & x_{-1} & x_{-2} & x_{-3} \\ x_3 & x_2 & x_1 & x_0 & x_{-1} & x_{-2} \\ x_4 & x_3 & x_2 & x_1 & x_0 & x_{-1} \\ x_5 & x_4 & x_3 & x_2 & x_1 & x_0 \end{bmatrix} \begin{bmatrix} C_{-3} \\ C_{-2} \\ C_{-1} \\ C_0 \\ C_1 \\ C_2 \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 1 \\ 1 \\ 0 \\ 0 \end{bmatrix} \tag{7}$$

where, $x_{-5} \sim x_5$ are the precursors and postcursors of channel pulse response which can be obtained by inversing Fourier transformation of the measured S-parameter, and vector $[\,0\ 0\ 1\ 1\ 0\ 0\,]^{\mathrm{T}}$ is the target of equalization. In this way, the optimal value $[\,C_{-3}\ C_{-2}\ C_{-1}\ C_0\ C_1\ C_2\,]^{\mathrm{T}}$ can be found[10].

3 Experimental results

The equalizer has been fabricated using 0.18μm CMOS process. Fig. 8 gives the die photograph of the chip which has an area of $0.68 \times 0.8\,\mathrm{mm}^2$ including I/O pads. An on-chip measurement is performed, in which the input of the chip is a 300mV 10Gb/s PRBS23 differential signal and its output is passed through an 18-inch FR4 backplane whose insertion loss is about 16.5dB at 5GHz, shown as Fig. 9.

After that, the output eye diagrams of a 46cm FR4 backplane are captured shown as Fig. 10. A duobinary signaling with a vertical eye opening of 45mV is constructed at the end of the channel, indicating that the design has successfully achieved a 10Gb/s duobinary signal over the FR4 backplane with 16.5dB losses at Nyqiust frequency. Table 1 compares the performance of the proposed 10Gb/s duobinary equalizer with other previous work[11-13]. The work can generate an eye opening of 45mV which is the maximum value among these work while its backplane insertion loss of 16.5dB is also the maximum one compared to the other three backplanes, at the cost of larger area and higher power consumption.

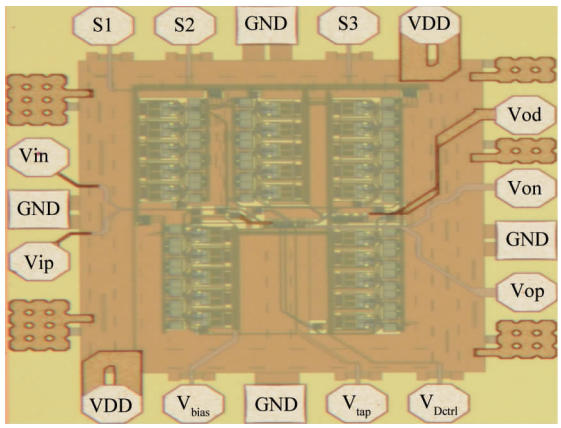

Fig. 8 Chip die photograph

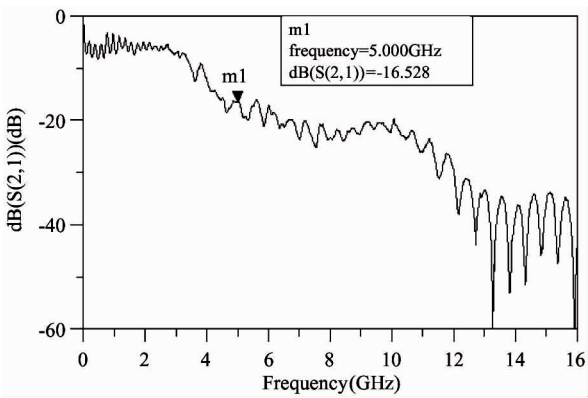

Fig. 9 Backplane Frequency response

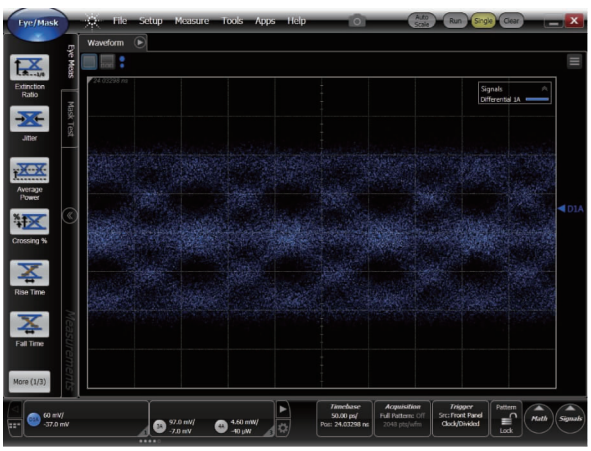

Fig. 10 Measured 10Gb/s eye-diagram after the equlizer and 18-inch backplane

Table 1 Performance summary and comparison

	The proposed work	Ref. [11]	Ref. [12]	Ref. [13]
Date Rate(Gb/s)	10	20	18	20
Process(CMOS)	180nm	90nm	90nm	90nm
Power supply(V)	1.8	1.5	1.2	1.5
Backplane	46cm FR4 PCB	10cm FR4 PCB	25cm low-ε PCB	16cm FR4 PCB
Insertion loss (dB) @ Nyquist Frequemcy	16.5	9.5	14	14.7
Eye Opening(mV)	45	35	43	30
Area(mm^2)	0.53	0.21	0.2	0.14
Power(mW)	194	120	N/A	81

4 Conclusion

In this study, a 10Gb/s transmit equalizer using duobinary signaling is realized based on 0.18μm CMOS process for FR4 backplane. With a 6-tap architecture and calibration technique, the equalization filter can acquire appropriate high-frequency gains and improve the flatness of group delay. Measurement results show that 10Gb/s 3-level duobinary eye diagrams with 45mV eye opening can be obtained over the 46cm FR4 backplane channel whose loss is up to 16.5dB at 5GHz.

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