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A wideband *LC*-VCO for MMMS applications①

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Abstract

A fully integrated wideband voltage-controlled-oscillator (VCO) based on current-reused topology is presented. The overall scheme contains two sub-VCOs, which are controlled by a switch to cover a wide output frequency range. Fabricated in TSMC 65 nm CMOS technology, the measured output frequency of the VCO ranges from 3.991 GHz to 9.713 GHz, achieving a tuning range of 83.5%. And the worst and best phase noise at 1 MHz offset are −93.09 dBc/Hz and −111.97 dBc/Hz, respectively. With a 1.2 V supply voltage, the VCO core consumes a current of 3.7 − 5.1 mA across the entire frequency range. The chip area is 0.51 mm^2, including the pads. Moreover, the proposed VCO provides a figure-of-merit-with-tuning-range (FOM_T) of −191 dBc/Hz to −197 dBc/Hz.

Key words: current-reuse, phase noise, voltage-controlled-oscillator (VCO), wideband

0 Introduction

Nowadays, the widespread of wireless communications increases the demand of integrating all the transceiver circuits, supporting the multi-mode and multi-standard (MMMS), in a single chip. Hence, the multi-mode multi-frequency (MMMF) wideband phase-locked loop (PLL), as one of the most important blocks in a multi-mode radio frequency (RF) transceiver system, has drawn researchers' attention extensively[1-3].

However, the bottleneck of realizing the wideband PLL frequency synthesizer is the design of the voltage-controlled oscillator (VCO)[4,5], which requires to be tunable consecutively in a wide frequency range.

Commonly, there are two kinds of VCOs, namely *LC*-VCO and ring oscillator VCO. However, as the *LC*-VCOs have a better phase noise performance than the ring oscillators, they are more preferred in the high-performance wideband PLL frequency synthesizer. But their achievable frequency tuning range (FTR) is usually limited by the low varactor ratio C_{max}/C_{min}. Therefore, the switched capacitors or switched inductors technologies[6,7] have been presented in the past decades to enhance the FTR. Moreover, the transformer-based resonators[8] that can generate two distinct frequency bands are exploited to realize the wideband VCOs. For this technique, care must be taken to implement the transformer, for example, we should design the two ports of the transformer to be placed on the same side to facilitate the connection with the capacitors and the two coils need to be coupled weakly[9]. Considering the on-chip inductor in the *LC*-tank covers a larger area, the tunable active inductor[10] was also adopted to improve the FTR of the VCO. However, this method worsens both the power consumption and the phase noise performance[11]. Thus, a fully integrated VCO is proposed, which is constituted by two current-reused-topology-based sub-VCOs, to achieve a broad frequency range and save the power consumption.

The rest of the paper is organized as follows. Section 1 describes the architecture of the VCO briefly. Then, Section 2 gives the detailed circuits design of each block. Next, the measured results are covered in Section 3. Finally, Section 4 presents the conclusion of the whole work.

1 Architecture of the proposed VCO

The architecture of the proposed VCO is shown in Fig. 1. As can be seen, it is composed of two sub-VCOs (VCO1 and VCO2), which are both based on the current-reused topology and controlled by a selecting signal *S*. When the signal *S* is 1.2 V, the MS1 is switched on and the MS2 is switched off, thus, the differential pairs MP1 and MN1 start to work, which gen-

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erate the negative resistance to compensate the loss of the *LC*-tank; on the contrary, if the signal *S* is 0, the MS2 is turned on and MS1 is turned off, which means that the negative resistance is provided by the differential pairs MP2 and MN2. For the two sub-VCOs, since their capacitor bank and varactors are the same, we can select a proper inductance for each of them to make they operate at two distinct frequency bands, namely the high frequency band and the low frequency band of the whole VCO. Note that, since the lossy switches MS1 and MS2 are added outside of the *LC*-tank, no phase noise degradation is caused by the switching process.

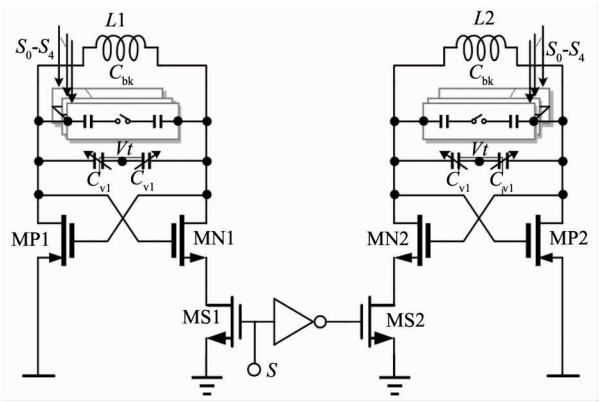


Fig. 1 Architecture of the proposed VCO

2 Circuit design

A 5-bit switched capacitor array, as shown in Fig. 2, is implemented to relieve the contradiction between the FTR and phase noise performance. The size of the switching transistors and the fixed capacitances in the array are both increased as the proportion of 1∶2∶4∶8∶16. When all the switching transistors are switched on, the switched capacitor array acquires the maximum capacitance, which can be calculated as

$$C_{\max} = (2^5 - 1)C_0/2 = 15.5C_0 \tag{1}$$

where C_0 is the unit capacitance used in the switched capacitor array. Then, switching off the whole switching transistors generates the minimum capacitance, which can be expressed as

$$\begin{aligned} C_{\min} &= \frac{1}{2}\left[\left(\frac{1}{C_0}+\frac{1}{C_p}\right)^{-1}+\left(\frac{1}{2C_0}+\frac{1}{2C_p}\right)^{-1}\right. \\ &\quad +\left(\frac{1}{4C_0}+\frac{1}{4C_p}\right)^{-1}+\left(\frac{1}{8C_0}+\frac{1}{8C_p}\right)^{-1} \\ &\quad \left.+\left(\frac{1}{16C_0}+\frac{1}{16C_p}\right)^{-1}\right] \\ &= 15.5\left(\frac{1}{C_0}+\frac{1}{C_p}\right)^{-1} \end{aligned} \tag{2}$$

where C_p is the unit parasitic capacitance when the switching transistor is turned off.

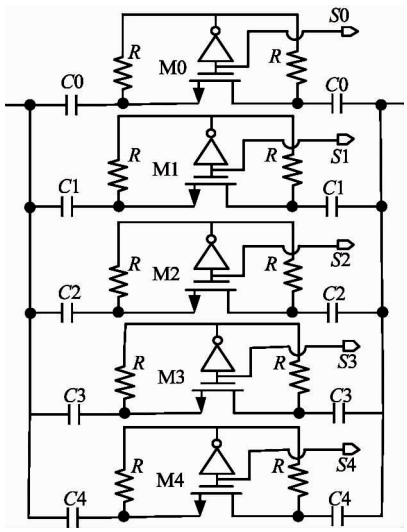


Fig. 2 Schematic of the 5-bit switched capacitor array

Then, the varactors are designed. Supposing the varactor's maximum and minimum capacitances are $C_{v,\max}$ and $C_{v,\min}$ respectively, in order to make the VCO's output frequency range be consecutive, Eq. (3) must be guaranteed:

$$C_{V,\max} - C_{V,\min} > C_0 - \left(\frac{1}{C_0}+\frac{1}{C_p}\right)^{-1} \tag{3}$$

Moreover, the output frequency of the VCO f_0 can be written as

$$f_0 = \frac{1}{2\pi\sqrt{L(C+C_{\text{var}})}} \tag{4}$$

where L, C_{var} and C represent the inductance, varactors and the rest capacitances respectively. Thus, the tuning gain K_{VCO} can be mathematically calculated as[12]

$$K_{\text{VCO}} = \left|\frac{\partial\omega}{\partial V_{\text{ctrl}}}\right| = \frac{L}{2}\omega^3\left|\frac{\partial C_{\text{var}}}{\partial V_{\text{ctrl}}}\right| \tag{5}$$

where V_{ctrl} is the control voltage of the varactors. From Eq. (5), it can be found that K_{VCO} varies with the output frequency. Furthermore, the steepness of the varactor results in that the output frequency of the VCO varies a lot over the voltage control range, which may degrade the performance of the VCO, such as stability and phase noise[13].

Thus, the distributed MOS varactor[13], as shown in Fig. 3, is adopted in this design. By biasing the MOS varactors with different voltages, the MOS varactors can provide a quasi-constant K_{VCO} over the whole tuning range[13]. In other words, a *C-V* curve with better linearity can be obtained. In order to observe the difference more intuitively, Fig. 4 illustrates the *C-V* curves of a single MOS varactor and the distributed MOS varactor simultaneously. As can be seen, the dis-

tributed MOS varactor with different biasing has a better linearity and a larger effective tuning range. When the linearity of the varactor is improved, the amplitude modulation-phase modulation (AM-PM) noise conversion of the VCO can be decreased, thus, a better phase noise performance can be obtained[13].

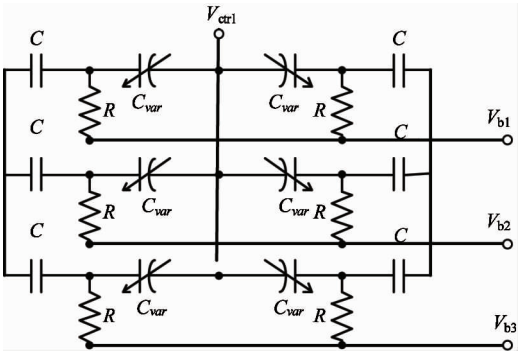


Fig. 3 Schematic of the distributed MOS varactor

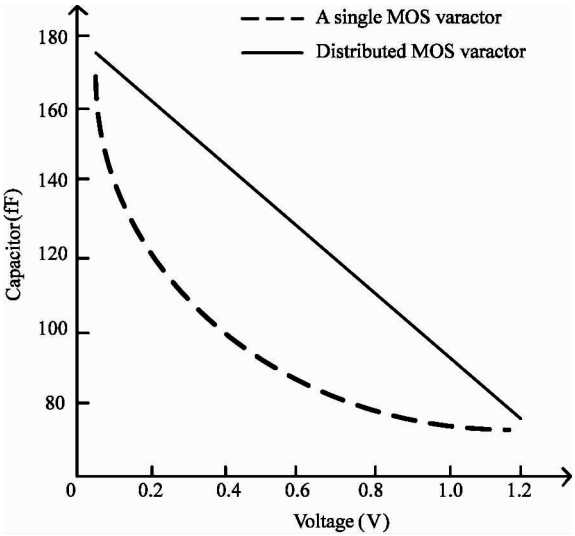
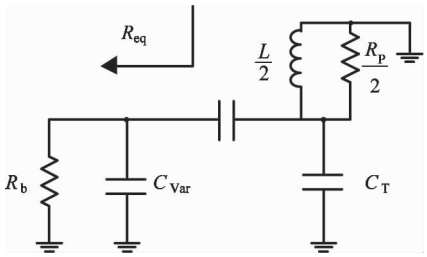


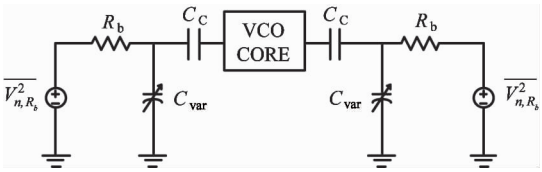
Fig. 4 *C-V* curves of MOS varactor

However, it should also be noted that, the biasing resistors of the distributed MOS varactor degrade the quality factor Q of the *LC*-tank and the thermo noise of the biasing resistors modulate the output frequency of the VCO, which both worsen the output phase noise to some extent. Hence, in order to select the proper biasing resistors, the simplified small-signal equivalent circuit of the *LC*-tank and the equivalent circuit of the biasing resistor noise when the control voltage equals 0, are presented in Fig. 5(a) and (b), respectively, where R_b, C_{var} and C_c represent biasing resistor, varactor and blocking capacitor, respectively, and $L/2$, $R_p/2$ and C_T are the inductor, the parallel resistor of the inductor and the parasitic capacitor of the *LC*-tank, respectively.

Observing Fig. 5 (a), from the right side of C_c,



(a) *LC*-tank



(b) Biasing resistor noise when the control voltage equals 0

Fig. 5 Simplified small-signal equivalent circuit

the equivalent impedance can be written as

$$R_{eq} = \left(1 + \frac{C_{var}}{C_C}\right)^2 R_b \tag{6}$$

When the blocking capacitor C_c satisfies $C_c \approx 10\ C_{var}$, it can be obtained:

$$R_{eq} \approx 1.2R_b \tag{7}$$

Therefore, in order to avoid degrading the quality factor of the *LC*-tank remarkably, the biasing resistor R_b should be at least 10 times of the parallel resistor of the inductor $R_p/2$.

On the other hand, the output phase noise caused by the thermo noise of the biasing resistor is calculated as

$$S_{\phi n}(f) = S_{ctrl}(f)\frac{K^2_{VCO}}{\omega^2} \tag{8}$$

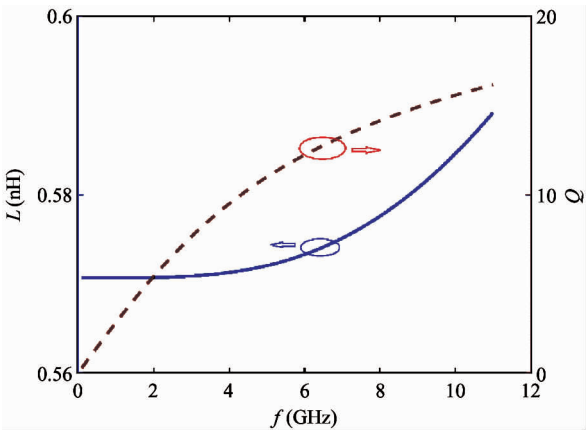
where S_{ctrl} is the noise spectrum of the control end. Since the gain of the thermo noise of the resistor to the output is $K_{VCO}/2$, the output phase noise can be derived as

$$S_{\phi n}(f) = \frac{kTR_bK^2_{VCO}}{4\pi^2 f^2} \tag{9}$$

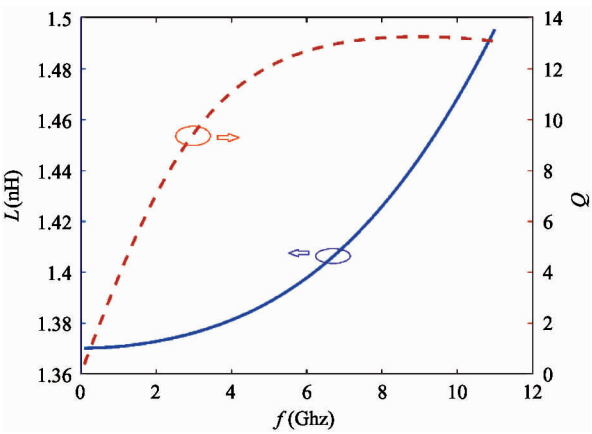
It shows that increasing the value of the biasing resistor degrades the output phase noise. Hence, in order to balance the quality factor of the *LC*-tank and the performance of the phase noise, we suggest setting $R_b = 10(R_p/2)$.

Next, let's start to design the inductors for the two sub-VCOs. Since the TSMC 65 nm CMOS technology provides an exact model for the inductor under 40 GHz and the proposed VCO works under 10 GHz, we can select the needed inductors from the technology library directly. After determining the maximum and minimum capacitance, including the switched capacitor array, the distributed MOS varactor and all the parasit-

ic capacitors, of the designed *LC*-tank, the required inductances for each sub-VCO can be obtained according to Eq. (4). Then, the required inductors can be selected from the TSMC PDK Inductor Finder. Finally, the L/Q curves of the selected inductors for high-band sub-VCO and low-band sub-VCO are shown in Fig. 6(a) and (b), respectively. Assuming that the high band is around 7 – 10 GHz and the low band is around 4 – 7 GHz, it can be found that, for the both inductors, the quality factors Q are both above 10 in the frequency range of interest.



(a) high-band sub-VCO



(b) low-band sub-VCO

Fig. 6 L/Q curves of the selected inductors

Finally, about the cross-coupled transistor pair, the current-reuse cross-coupled transistor pair[14], which is half of the conventional NMOS/PMOS cross-coupled transistor pair, as shown in Fig. 7, is adopted.

In the working process, the PMOS and NMOS transistor are turned on/off simultaneously. In the first half of the oscillation period, the PMOS and NMOS transistors are turned on, the current flows through the PMOS, *LC*-tank and the NMOS to the ground, note that, when the output voltage swing approaches the peak value, the NMOS and PMOS work in the linear region,

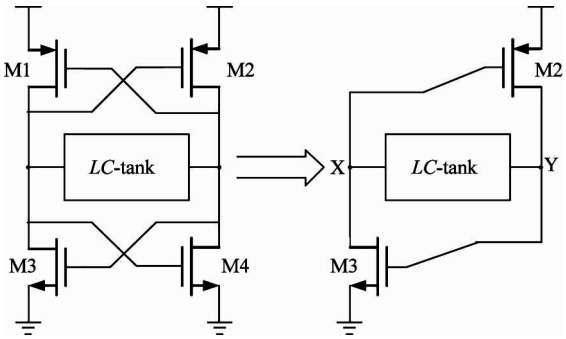


Fig. 7 Architecture of the current-reused cross-coupled transistor pair

which means the voltage swing is limited by the supply voltage, i. e. the VCO is in the voltage-limited region; While in the second half of the oscillation period, the PMOS and NMOS transistors are both turned off, the current flows through the capacitances at nodes X and Y to the ground, in this case, the output voltage swing can be higher than the supply voltage, instead of being limited by the supply voltage. Thus, the output voltage waveform of the VCO suffers from the asymmetric distortion, which worsens the output phase noise to some extent. In order to improve the symmetry of the output waves in the two half-periods, the extra resistors are adopted to bias the transistors in the current-limited region[15]. However, considering the thermo noise of the added resistors, the phase noise improvement is limited, and this method increases the size of the cross-coupled transistors, which decreases the working frequency of the VCO. Thus, the classic current-reuse cross-coupled transistor pair architecture, as presented in Fig. 1, is adopted in the design.

Compared with the conventional cross-coupled transistor pair, such as the NMOS cross-coupled transistor pair, PMOS cross-coupled transistor pair and the PMOS/NMOS cross-coupled transistor pair, the current-reuse architecture provides the following three advantages. First, it can save about half of the current consumption while providing the same negative resistance. Secondly, as there is no common-source node, the phase noise can be avoided being degraded by the second-harmonic terms. Lastly, since less transistors connected to the resonator guarantees lower parasitic capacitances, it can improve the working frequency range[11].

3 Measured results

The proposed VCO is implemented in TSMC 65 nm CMOS process. The chip covers an area of 0.51 mm^2, including the pads, and the microphotograph of the

chip is presented in Fig. 8. The performance of the fabricated VCO is evaluated on wafer by using a Cascade Microtech probe station. The output spectra and phase noise of the VCO are measured by an Agilent E4440A spectrum analyzer.

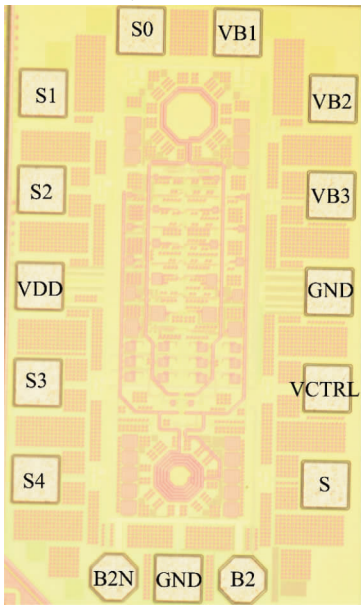


Fig. 8 Microphotograph of the chip

Fig. 9 shows the measured tuning curves of the proposed VCO. As can be seen, the proposed VCO can be tuned from 3.991 GHz to 9.713 GHz consecutively, and a tuning range of 83.5% is achieved. Moreover, the output spectra and phase noise of the VCO at 9.713 GHz and 3.991 GHz are shown in Fig. 10 (a), (b), (c) and (d), respectively. Fig. 10 (c) and (d) state that the best and the worst phase noise of the proposed VCO at 1 MHz offset are −93.09 dBc/Hz and −111.97 dBc/Hz, respectively.

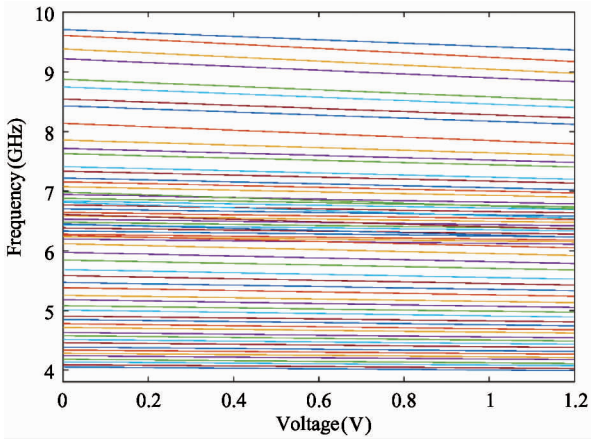
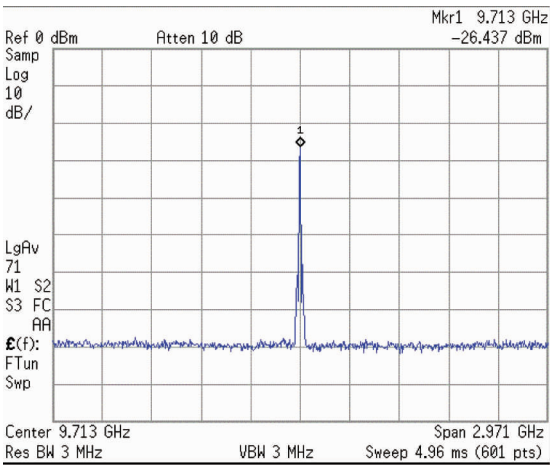
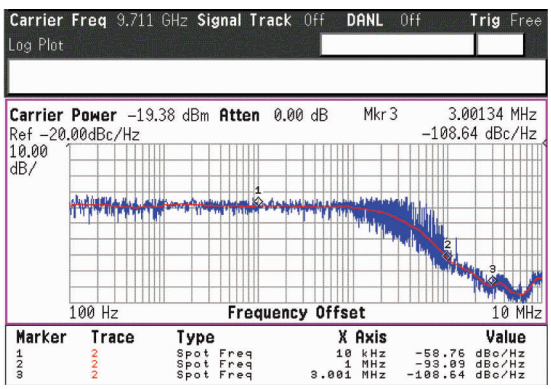


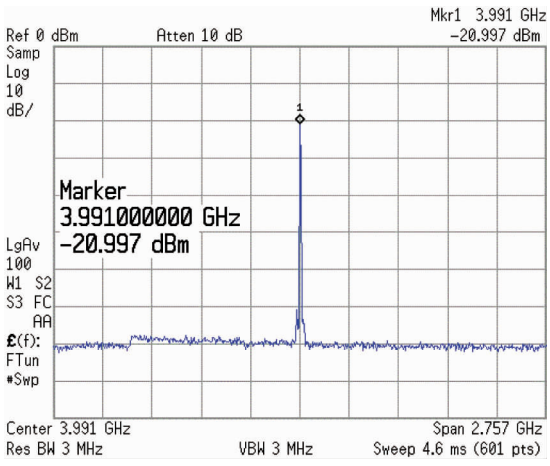
Fig. 9 Measured tuning curves of the proposed VCO



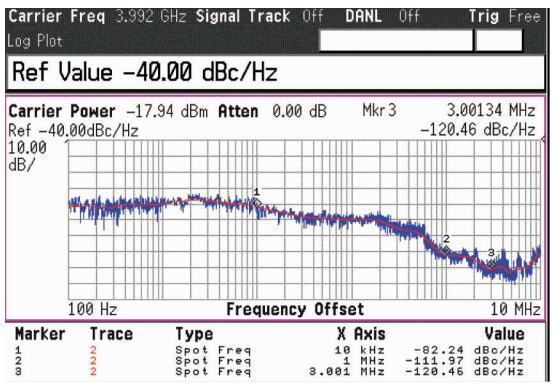
(a) Output spectrum at 9.713 GHz



(b) Phase noise at 9.713 GHz



(c) Output spectrum at 3.991 GHz



(d) Phase noise at 3.991 GHz

Fig. 10 Output spectra and phase noise of the VCO

Normally, the figure-of-merit-with-tuning-range (FOM_T)[16] is defined as

$$FOM_T = L(\Delta f) + 10\log\left(\frac{P_{DC}}{1\text{mW}}\right) - 20\log\left(\frac{f_{osc}}{\Delta f}\right) - 20\log\left(\frac{TR(\%)}{10}\right) \quad (10)$$

where, $L(\Delta f)$ is the phase noise of an offset-frequency of Δf, P_{DC} is the DC power consumption, f_{osc} and TR represent the oscillation frequency and the tuning range, respectively. Thus, it can be derived that the proposed VCO provides an FOM_T of −191 dBc/Hz to −197 dBc/Hz. Finally, The VCO performance is summarized and compared with state-of-the-art VCOs in Table 1.

Table 1 VCO performance summary and comparison

References	CMOS(nm)	Frequency (GHz)	$TR(\%)$	P_{DC}(mW)	Phase noise (dBc/Hz)	FOM_T (dBc/Hz)
[16]	65	6.2	16.1	4.32	−119.2@1MHz	−192.9
[17]	65	2.9	35	0.33	−121.6@1MHz	−205.4
[18]	65	3.9	10.2	25.8	−131.6@1MHz	−190
This work	65	6.9	83.5	5.1	−111.97@1MHz	−197

4 Conclusion

A fully integrated wideband VCO is presented, which is based on the current-reused topology. The overall scheme contains 2 sub-VCOs, which are controlled by a switch to cover a wide output frequency range. In each sub-VCO, a 5-bit switched capacitor array and distributed MOS varactor are adopted to tune the output frequency consecutively. Fabricated in TSMC 65 nm CMOS technology, the measured results show that the output frequency range of the VCO is 3.991 − 9.713 GHz, achieving a tuning range of 83.5%. And the worst and best phase noise at 1 MHz offset are −93.09 dBc/Hz and −111.97 dBc/Hz, respectively. Furthermore, the VCO core draws a current of 3.7 −5.1 mA from a 1.2 V supply voltage across the entire frequency range. The chip area is 0.51 mm^2, including the pads. Finally, the FOM_T of the proposed VCO is from −191 dBc/Hz to −197 dBc/Hz.

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