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A compact and reconfigurable low noise amplifier employing combinational active inductors and composite resistors feedback techniques①

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Abstract

A compact and reconfigurable low noise amplifier (LNA) is proposed by combining an input transistor, composite transistors with Darlington configuration as the amplification and output transistor, T-type structure composite resistors instead of a simplex structure resistor, a shunt inductor feedback realized by a tunable active inductor (AI), a shunt inductor peaking technique realized by another tunable AI. The division and collaboration among different resistances in the T-type structure composite resistor realize simultaneously input impedance matching, output impedance matching and good noise performance; the shunt feedback and peaking technique using two tunable AIs not only extend frequency bandwidth and improve gain flatness, but also make the gain and frequency band can be tuned simultaneously by the external bias of tunable AIs; the Darlington configuration of composite transistors provides high gain; furthermore, the adoption of the small size AIs instead of large size passive spiral inductor, and the use of composite resistors make the LNA have a small size. The LNA is fabricated and verified by GaAs/InGaP hetero-junction bipolar transistor (HBT) process. The results show that at the frequency of 7 GHz, the gain S_{21} is maximum and up to 19 dB; the S_{21} can be tuned from 17 dB to 19 dB by tuning external bias of tunable AIs, that is, the tunable amount of S_{21} is 2 dB, and similarly at 8 GHz; the tunable range of 3 dB bandwidth is 1 GHz. In addition, the gain S_{21} flatness is better than 0.4 dB under frequency from 3.1 GHz to 10.6 GHz; the size of the LNA only has 760 μm × 1260 μm (including PADs). Therefore, the proposed strategies in the paper provide a new solution to the design of small size and reconfigurable ultra-wideband (UWB) LNA and can be used further to adjust the variations of gain and bandwidth of radio frequency integrated circuits (RFICs) due to package, parasitic and the variation of fabrication process and temperature.

Key words: variable gain, variable bandwidth, low noise amplifier (LNA), resistance feedback, tunable active inductor (AI)

0 Introduction

Low noise amplifier (LNA) is an important module of receiver front-end. With the increasing requirement for high performance of a receiver from customers, the LNA is inevitably desired to have high gain, wide frequency-band and wide tunability, also small size to accommodate miniaturization of the receiver[1]. To realize impedance matching in wide frequency-band, obtain good noise performance, boost gain and extend frequency bandwidth, it is common to adopt passive spiral inductor (PSI) degeneration technique and inductor peaking technique. However, the PSIs occupy a large proportion of the chip area due to the large size of PSI. For example, for a LNA designed by Ham et al.[2] based on PSIs, the consumed area of PSIs is four-fifths of the whole area of the chip. Instead of large size of PSI, the feedback resistance technique is easy to implement and is always employed[3-5]. However, a simplex structure feedback resistor is difficult to simultaneously meet the requirement for impedance matching and good noise of LNA. In the design of a LNA, in order to boost gain, the Darlington configuration of composite transistors, in which emitter of one transistor drives the base of another transistor, is a good method due to its high gain compared with a low gain of one stage transistor. But the only adoption of

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simple Darlington configuration of transistors does not achieve good flatness of gain of LNA. For example, for a two-stage 1 – 8 GHz Darlington LNA designed by Kevin et al. [6], the power gain is as high as 17.5 dB, the minimum noise factor is 2.5 dB, but the flatness of gain is poor. In addition, the gain of LNA is expected to be tuned to accommodate the variation of a strong or weak input signal and to meet the requirement of gain adjustment. The tunable style of gain can be divided into discrete and continuous modes. The commonly tuned gain methods include a variable transconductance of transistor[7-8], a current-steering technique[7,9], a variable load resistance[7,10], an operational-amplifier based method[11] and frequency-translated (FT) impedance method[12]. However, these methods not only degrade noise and matching performance but also limit the bandwidth (BW), and the use of the array cells further increases design complicity and chip size.

In this paper, a combination technologies of a T-type composite resistors structure instead of a simplex resistor structure, a Darlington configuration of composite transistors, a shunt tunable active inductor (AI) feedback and a shunt AI peaking technique is employed to simultaneously realize input impedance matching, output impedance matching, optimize noise performance, boost gain, extend frequency bandwidth and improve the gain flatness of a LNA by taking full advantages of division and collaboration of these various technologies. Furthermore, the small size of the chip can be achieved due to the absence of large size passive spiral inductor (PSI), and the gain and 3 dB frequency bandwidth can be adjusted by tuning external bias of shunt feedback AI and shunt peaking AI. Finally, the proposed LNA is fabricated and verified based on GaAs/InGaP hetero-junction bipolar transistor (HBT) process. The strategy used in this paper provides a solution to the design of LNA with small size, high gain, wide tunable range of gain and bandwidth.

1 The topology of the proposed LNA and the fabrication process flow

The topology of the proposed low noise amplifier is shown in Fig. 1.

The proposed LNA mainly consists of an input transistor Q_{21}, composite transistors of Q_{22} and Q_{23} with Darlington configuration as output transistors, local shunt inductor feedback circuit branch constituted by a resistor R_1 and an active inductor (AI1) in series, shunt inductor peaking circuit branch constituted by a load resistor R_L and another active inductor (AI2) in series, and T-type composite resistors constituted by

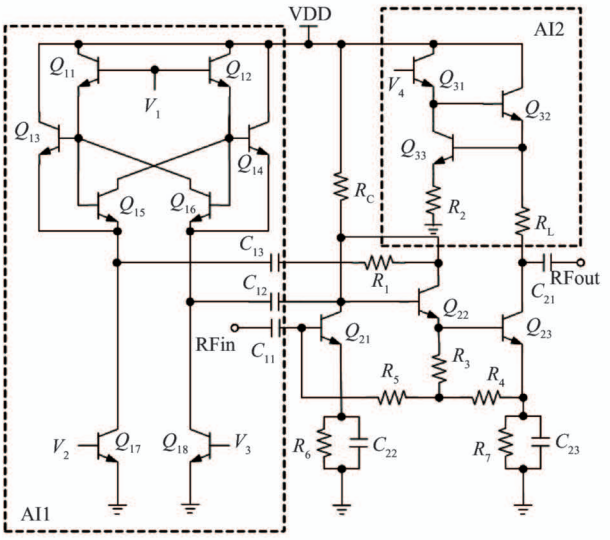

Fig. 1 Circuit topology of the proposed LNA with tunable active inductors, T-type composite resistors and Darlington composite transistors

R_3, R_4 and R_5. In addition, VDD is a power supply; R_c is a load resistor of Q_{21}; C_{11}, C_{12}, C_{13} and C_{21} are DC blocking capacitors; C_{22} and C_{23} are bypass capacitors, and R_6 and R_7 are emitter feedback resistors of transistor Q_{21} and Q_{23} respectively.

The base of input transistor Q_{21} is radio frequency (RF) signal input port terminal of the LNA; Q_{22} and Q_{23}, in which the emitter of the Q_{22} drives the base of Q_{23}, are Darlington configuration to amplify the signal and achieve high gain compared with a low gain of one stage transistor, and the collector of Q_{23} serves as RF signal output port terminal of the LNA.

In contrast with a simplex structure resistance feedback in the traditional LNA, in the proposed LNA, the T-type composite resistors constituted by R_3, R_4 and R_5 are introduced skillfully among Q_{21}, Q_{22} and Q_{21} by division and collaboration style. On the one hand, R_5 as feedback resistance between Q_{21} and Darlington transistors provides base current for transistor Q_{21}, on the other hand, $R_5 - R_4$ and $R_5 - R_3$ constitutes system overall feedback loop and local feedback loop respectively. As a result, the cooperation among R_3, R_4 and R_5 in T-type resistors structure can simultaneously realize input and output impedance matching, and optimize the noise of the LNA.

The local shunt inductor feedback circuit branch constituted by R_1 and AI1 in series is used to stabilize base bias of Q_{22}, to increase gain at high frequency and improve the flatness of gain; the shunt inductor peaking circuit branch constituted by R_L and another AI2 in series is used to stabilize collector bias of Q_{22} and Q_{23}, to increase zero poles, hence extend frequency

bandwidth, and improve output impedance matching in conjunction with resistor R_3.

Furthermore, the use of two tunable AIs in this LNA instead of passive spiral inductors (a feedback inductor and a peaking inductor) can not only save chip area but also tune gain and bandwidth of LNA simultaneously by tuning inductance value of two tunable AIs (AI1 and AI2).

Based on 0.2 μm GaAs/InGaP HBT process, the main fabrication steps of the LNA integrated circuit (IC) chip are as follows: the etch of the emitter, base and collector metal fingers, and their mesas, the etch of thin-film resistor (TFR), the etch of first interconnection metal and second interconnection metal, the etch of first via and second via, the etch of protective layer and pad, as shown in Fig. 2.

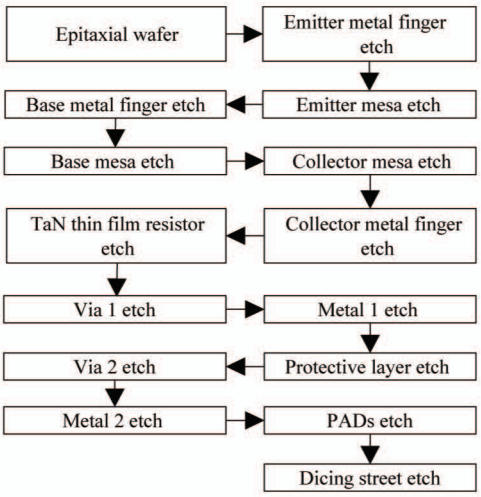

Fig. 2 The fabrication process flow chart of monolithic integrated LNA circuit chip

The process flow aims to fabricate LNA in the dry etching method so as to get rid of the traditional wet etch method and realize the fabrication of the passive components such as TaN film resistors and metal-insulator-metal (MIM) capacitor, and active HBTs devices simultaneously. In this way, the line strip integrity of the emitter finger and the base finger can be preserved due to the minimization of lateral etch. Furthermore, as another feature of the process compared with the traditional process, instead of the dielectric layer, the emitter metal film, base metal film, collector metal film and photo-resist film are acted as the protective layer of the active region during the etching. Therefore the fabrication steps are decreased, and the fabrication success possibility is increased. In addition, the two layers interconnect metal and two via technologies are also employed to minimize parasitic resistance and capacitance, and decrease the LNA chip size.

2 Results and discussions

The photomicrograph of the fabricated LNA integrated circuit chip is shown in Fig. 3. The size, including bias, signal and ground PADs, is 760 μm × 1260 μm. On the top side of the chip, there are 6 PADs, which are tuning port of V_1, V_2, V_3 and V_4 of two tunable AIs (AI1 and AI2), power supply V_{DD} and ground respectively. On the left side of the chip, the PAD is a RF signal input port; the RF signal output PAD is on the right side of the chip. The key circuit parameters are as follows. For transistors Q_{21}, Q_{22} and Q_{23}, the sizes of emitter finger, base finger and collector finger are 2 μm × 40 μm, 1 μm × 44 μm and 10 μm × 47 μm, and the finger number are 3, 4 and 2, respectively. The resistance values of R_1, R_2, R_3, R_4, R_5, R_6, R_7 and R_L are 520 Ω, 4 Ω, 60 Ω, 400 Ω, 320 Ω, 5 Ω, 11 Ω and 50 Ω.

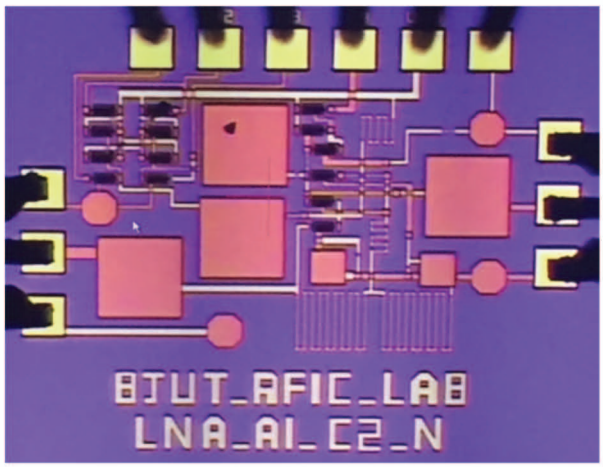

Fig. 3 Chip photomicrograph of the proposed LNA under measurement

On-chip S parameters and noise factor measurement of the LNA are performed by means of 150 μm pitch GSGSG Cascade Summit 12 000 probe station. The instruments used in this measurement include Agilent vector network analyzer PNA N5320A, noise factor analyzer N8975A, ENR noise source, high-speed DC power supply E5260A, attenuator, WR15 waveguide adapter, DC blocker from SHF. SOLT calibration is performed by means of a 104-783A GSG substrate and WinCal XE software by cascade.

The gain S_{21} versus frequency for the LNA under four combined bias V_{Bias} of two tunable AIs (AI1 and AI2) is shown in Fig. 4. The correspondence between the combined bias V_{Biasi} (i = 1, 2, 3, 4) and tuning port bias V_i (i = 1, 2, 3, 4) of two tunable AIs is listed in Table 1. It can be seen that at the frequency of 7 GHz, the gain S_{21} is maximum and up to 19 dB; the

gain can be tuned by changing external biases of two tunable AIs, for example, the S_{21} can be tuned from 17 dB to 19 dB at 7 GHz when the bias is adjusted from Bias4 to Bias3, that is, the tunable amount of S_{21} is 2 dB, and similarly at 8 GHz; in addition, the gain S_{21} flatness can also be improved by tuning external biases of two tunable AIs, for an example, in the frequency range from 3.1 to 10.6 GHz, the flatness of the gain S_{21} is better than 0.4 dB under Bias2, and is improved compared with that under Bias3 at the expense of the decrease of gain by 1.1 dB.

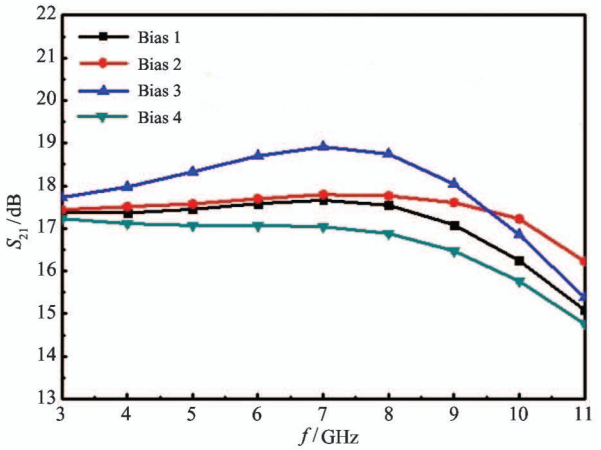

Fig. 4 Gain S_{21} versus frequency for the proposed LNA under different biases

Table 1 Voltage values of tuning ports for active inductors under various biases

	V_1	V_2	V_3	V_4
V_{Bias1}/V	3.83	1.37	1.37	3.51
V_{Bias2}/V	3.82	1.34	1.34	3.56
V_{Bias3}/V	3.85	1.33	1.33	3.58
V_{Bias4}/V	3.89	1.33	1.33	3.68

Fig. 5 shows the S_{21} versus frequency for the LNA under another two combined biases of V_{Bias5} (V_1 = 3.86 V, $V_2 = V_3 = 1.34$ V, $V_4 = 3.57$ V) and V_{Bias6} (V_1 = 3.89 V, $V_2 = V_3 = 1.37$ V, $V_4 = 3.63$ V) of two tunable AIs (AI1 and AI2). As shown, the gains are higher than 10.8 dB, and the 3 dB bandwidth range is 3 – 12 GHz under the bias of V_{Bias6}, the gains are greater than 12.4 dB and 3 dB bandwidth range is 2 – 12 GHz under the bias of V_{Bias5}, that is, the tunable range of 3 dB bandwidth is 1 GHz. The ability for LNA to tune gain and frequency bandwidth in this paper can be used to compensate for the degradation of gain and frequency due to package, process and temperature variation.

Fig. 6 shows the reverse gain of S_{12}, input return loss S_{11}, output return loss S_{22} of the LNA versus frequency f. In the frequency range from 3.1 to 10.6 GHz, S_{12} is better than −40 dB, the LNA has sound reverse isolation; $S_{11} < -14$ dB and $S_{22} < -11$ dB, the LNA has good input and output impedance matching.

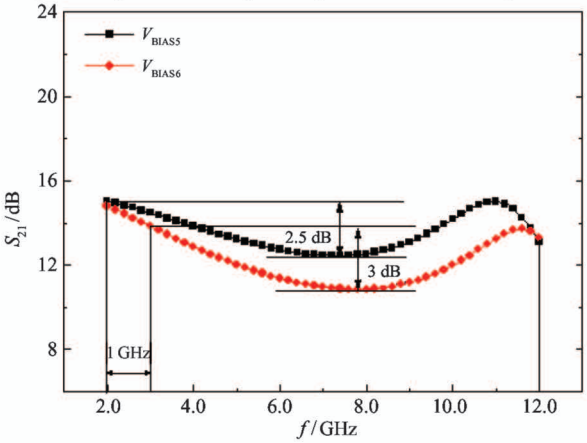

Fig. 5 Gain S_{21} versus frequency for the proposed LNA under two biases

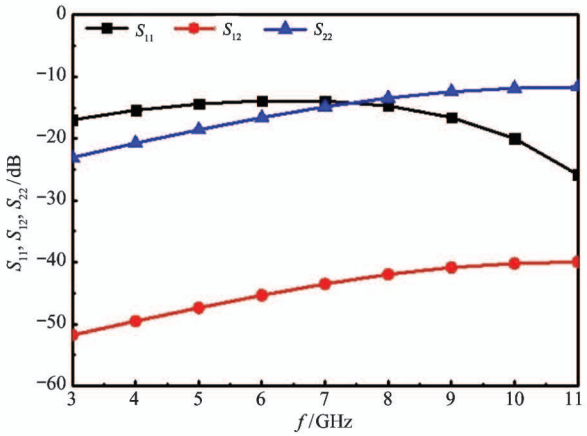

Fig. 6 S_{11}, S_{22} and S_{12} versus frequency for the proposed LNA

Fig. 7 shows the noise factor (NF) of LNA versus frequency. In the whole frequency band, the *NF* is less than 3.8 dB, and the good *NF* is achieved. The *NF* increases from 2.4 to 3.7 with frequency. This is a result mainly from the degradation of the noise performance of

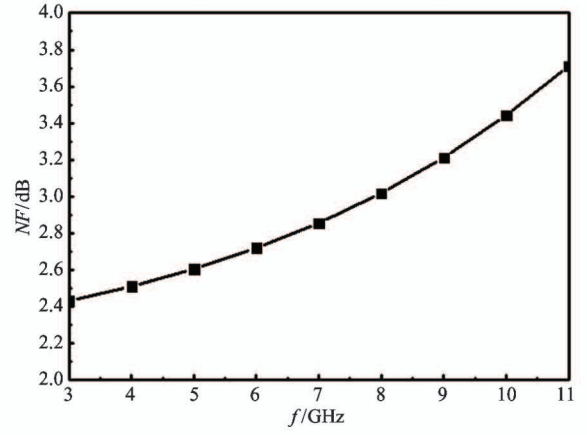

Fig. 7 Noise factor of the proposed LNA

active devices with frequency.

The comparison of the main performance parameters between the proposed LNA with published LNAs in recent years is listed in Table 2. It can be seen that the proposed LNA has some advantages in not only the simultaneous tunability of the 3 dB frequency bandwidth and gain under high frequency, but also the frequency range over published LNAs in recent years.

Table 2 Performance comparison between the proposed LNA with some recent studies

References	This work	Ref. [13]	Ref. [14]	Ref. [15]
Year	2020	2019	2018	2018
Frequency/GHz	3.1 – 10.6	2.4	3 – 12	7
Tunable frequency/GHz	1	NA	NA	NA
Gain/dB	15.5 – 19	15.2	19.2 – 20.2	6.7
Tunable gain/dB	2@8GHz	NA	NA	2.2
Noise/dB	2.4 – 3.7	2.17	1.72 – 1.99	6.1

3 Conclusions

A compact and reconfigurable LNA is realized by taking full advantages of division and collaboration of the combined technologies of a Darlington configuration of composite transistors, a T-type structure of composite resistors instead of a simplex resistor structure, a shunt inductor feedback realized by a tunable AI and a shunt inductor peaking technique realized by another tunable AI. The strategies of the use of small size and the tunable AIs instead of passive spiral inductors and T-type composite resistors instead of a simplex structure resistor used in the paper not only can realize simultaneously gain and frequency band performance tunability (reconfiguration) of LNA, which can be used to compensate the degradation of gain and frequency of LNA due to package, process and temperature variation, but also can save chip area. Therefore, this work provides a new solution to the design of small size and reconfigurable ultra-wideband LNA.

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