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Verilog HDL modeling and design of 10Gb/s SerDes full rate CDR in 65nm CMOS①

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Abstract

Phase locked loop (PLL) is a typical analog-digital mixed signal circuit and a method of conducting a top level system verification including PLL with standard digital simulator becomes especially significant. The behavioral level model (BLM) of the PLL in Verilog-HDL for pure digital simulator is innovated in this paper, and the design of PLL based clock and data recovery (CDR) circuit aided with jitter attenuation PLL for SerDes application is also presented. The CDR employs a dual-loop architecture where a frequency-locked loop acts as an acquisition aid to the phase-locked loop. To simultaneously meet jitter tolerance and jitter transfer specifications defined in G. 8251 of optical transport network (ITU-T OTN), an additional jitter attenuation PLL is used. Simulation results show that the peak-to-peak jitter of the recovered clock and data is 5.17ps and 2.3ps respectively. The core of the whole chip consumes 72mA current from a 1.0V supply.

Key words: Verilog-HDL, behavioral level model (BLM), phase locked loops(PLL), clock and data recovery (CDR)

0 Introduction

Clock and data recovery (CDR) is a critical function in high-speed transceivers. Such transceivers serve in many applications, including optical communications and chip-to-chip interconnects. Data received in these systems are both asynchronous and noisy, requiring that a clock is extracted to allow synchronous operations. Furthermore, the data must be "retimed" such that the jitter accumulated during transmission is removed. CDR circuits operating at tens of gigabits per second pose difficult challenges with respect to device, speed, jitter, signal distribution, system architecture, and power consumption[1].

This paper dedicates a design of a 9.95 ~ 11.5Gb/s full rate CDR with jitter attenuation PLL in 65nm CMOS technology that fulfills all of jitter specifications recommended by G. 8251. Jitter characteristics critical to G. 8251 recommendations are jitter transfer (bandwidth and jitter peaking), jitter tolerance, and jitter generation. With the development of the function and scale of IC, most integrated circuits realizations include both digital and analog functions. While the method of conducting the top level system verification including the PLL with the standard digital simulator has not been developed.

This paper presentes the method of behavioral level model for the PLL modules in Verilog-HDL in Section 1. In Section 2, the jitter specifications of G. 8251 are analyzed and the CDR architecture is introduced. Section 3 describes the building blocks and circuit design. Then, the post simulation results of CDR and jitter attenuation PLL circuits are given in Section 4. Section 5 summarizes the post simulation results and implementation details.

1 Behavioral level model of PLL

The behavioral level model aims to provide a behavioral model of all the blocks within the top level module, enabling designers to verify the increasingly complex design using a standard digital simulator, such as Verilog-XL and Modelsim. Several challenges arise in creating an accurate BLM in Verilog-HDL, and the most is due to Verilog's inherent inability to model and simulate currents and voltages. To overcome these obstacles, a virtual high frequency clock is created to

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perform discrete time simulation. The simulator treats all voltage and current values as real Verilog variables and samples or updates their values on the edge of the virtual clock. The clock provides necessary time increment to update the critical currents and voltages within the analog circuits that allow the BLM to model the real circuit accurately.

For example, charge and discharge current from the charge pump can be sampled by the virtual high-frequency clock as shown in Fig. 1, so the time-domain integration function of the LPF can be transformed to time-domain for the reason of the discretization of integrant. The output voltage of *LPF* is also discrete because it is the summation of that of the resistor R_P and capacitor *C*1. It can be described by the Verilog as follows:

```
always@ (posedge Sample _ clk)
begin
Iout = 'CHARGEPUMP _ I * ((UP < DN)?
( -1.0) : (UP-DN));
end
always@ (posedge Sample _ clk)
  begin
    Vc _ pre = Vc;
    Vc = Vc _ pre + Iout * (1/(2 * 'PI * 'SAM-
    PLE _ FREQ * 'C1));
    Vctrl = Vc + Iout * 'Rp;
  end
```

In which CHARGEPUMP _ I is the charge and discharge current of the charge pump, Vc is the voltage of capacitor, and SAMPLE _ FREQ is the frequency of the sampling clock.

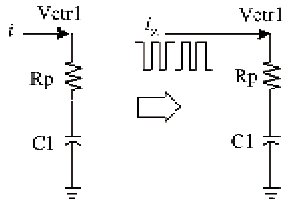

Fig. 1 The discretization of the time-domain integration

Fig. 2 shows the evolution procedure of the output frequency of VCO. Once the output voltage of LPF is generated, the corresponding oscillation frequency of the VCO can be deduced by the gain K_{VCO} of the VCO. Then the delay time and output frequency will be calculated by a forever function.

Fig. 3 shows the simulation results of the top level verification using a Modelsim simulator. As can be seen in the picture, the control-line of VCO exhibits the track and acquisition process during normal operation.

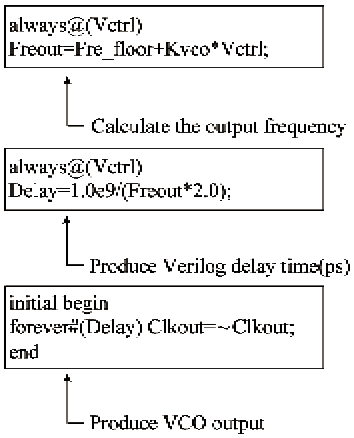

Fig. 2 The evolution procedure of VCO output frequency

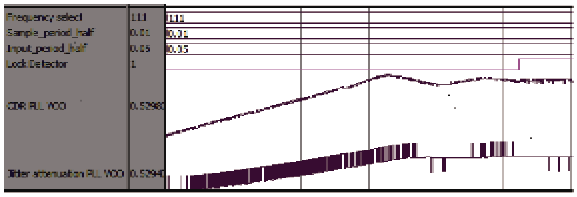

Fig. 3 Simulation results of the top level verification in Modelsim

2 Jitter analyses and CDR architecture

The jitter performance of a CDR is commonly characterized by jitter generation, jitter transfer and jitter tolerance. Normally, jitter tolerance and jitter generation are the performance requirements for high speed link CDRs which are used in chip-to-chip communication, and it does not need to meet jitter transfer specification. However, for those applications where the CDR is used in a repeater, as the case in SONET (synchronous optical network) systems, all the three jitter performances are needed[2].

Jitter transfer function of a CDR circuit represents that how much jitter passes through the system from its input to its output. There are two difficult specifications in jitter transfer. One is bandwidth, and the other is jitter peaking. The amount of jitter peaking must be less than 0.1dB. In order to meet the requirement of little jitter peaking, a damping factor above 4 ~ 6 must be adopted.

G.8251[3] defines the masks for OTU2 jitter tolerance and jitter transfer. It is important to note that the 0.15UI corner of jitter tolerance mask is at 4MHz, while the −3dB corner frequency of jitter transfer curve is 1MHz. In order to meet the jitter tolerance mask, the CDR PLL must be designed as that the closed-loop bandwidth is higher than the 0.15UI corner frequency of jitter tolerance. However, in this case, the CDR loop cannot meet jitter transfer mask. So these requirements suggest that a single CDR loop can-

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not be designed to meet jitter tolerance and jitter transfer mask[4] simultaneously.

In this design, a standard CDR PLL focusing on meeting jitter tolerance and an additional low-pass filter called jitter attenuation PLL for jitter transfer are introduced. Fig. 4 depicts the functional block diagram of the proposed clock and data recovery architecture. The data input is expected to be a non-return-to-zero (NRZ) data pattern at a rate between 9.95 and 11.5Gb/s. The CDR PLL employs a dual-loop architecture where the frequency-locked loop acts as an acquisition aid to the phase-locked loop and is disengaged during normal operation when the CDR PLL is locked to the input serial data. Thus the structure realizes a large frequency acquisition range, while maintaining the precise control of phase alignment to achieve the ITU-T OTN G.8251 jitter tolerance requirements. A conventional charge-pump based design is used and it is shared by the dual-loop.

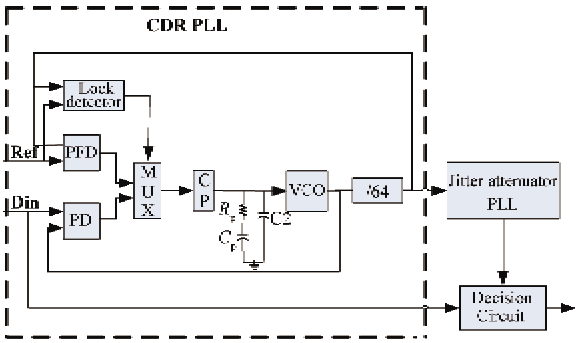

Fig. 4 The architecture of the proposed CDR

The proposed CDR implements a full-rate architecture because of its simplicity and robustness with regard to various data patterns. In full-rate CDR, the design of the voltage-controlled oscillator is simplified and the physical layout of CDR can be very dense to minimize parasitic, which in turn helps to improve speed and reduce noise coupling. In addition, the full-rate CDR generates a low jitter full-rate clock which is applied to retime the data from the input.

By the behavioral level simulation of VHDL model and the above CDR architecture, the design specifications of the module of CDR can be distributed. According to the tuning range of VCO and low control voltage range lead by low supply voltage of 65nm CMOS technology, the gain K_{VCO} is set to 600MHz. The −3dB bandwidth K of CDR is 4MHz, and the −3dB bandwidth of the Jitter attenuator PLL is 1MHz. The current I_P of charge pump is 80μA. Therefore, the R_p and C_p parameter of LPF can be calculated from Eq. (1) and Eq. (2).

$$R_p = \frac{2\pi K}{I_p \cdot K_{VCO}} \tag{1}$$

$$C_p = \frac{4\zeta^2}{K \cdot R_p} = \frac{2I_P K_{VCO}\zeta^2}{\pi K^2} \tag{2}$$

3 Building blocks and circuit design

3.1 Phase detector

Operating the Hogge detector at 10Gb/s is challenging when the key issues are achieving a low phase offset between the input clock and data signals (in order to achieve high jitter tolerance), and achieving a linear phase error characteristic over a wide phase error range. To address these issues, a buffer is inserted between the input data signal and the leftmost XOR gate input as shown in Fig. 5. The buffer is designed to have a delay that compensate for the clock-to-Q delay of the first register. Appropriate layout techniques is applied to achieve good matching since mismatch would contribute to phase offset in the overall phase detection operation.

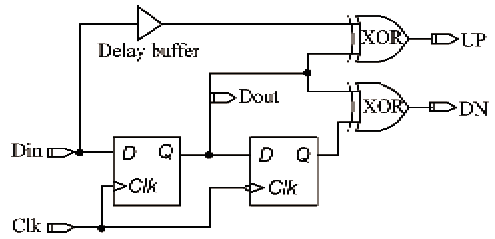

Fig. 5 Hogge phase detector

In this full-rate PD the sampling D flip-flop is the most critical building block, which has to track and sample the incoming 10Gb/s signal. So current-mode logic (CML) master-slave flip-flop is employed to meet the speed requirement.

The CML circuits have a higher immunity to supply noise and generate less switching noise on the power supply. In fact, the attainable data rate in CML flip-flop circuit is limited by the RC time constants of the circuit. Thus, optimizing the performance of the high speed CML flip-flop circuit becomes an exercise of minimizing these RC time constants.

3.2 Charge pump

As can be seen in Fig. 6, the charge pump is a completely active differential design with a common-mode feedback circuit. Due to jitter-related considerations (low noise and jitter peaking <0.1dB) and the practical size limitations for on-chip capacitors, the employed passive RC filter is a differential off-chip filter. Low-noise design makes it necessary to run a fairly

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high current in the charge pump. However, considering the relatively low power supply voltages of 65nm CMOS technology, careful optimization of the charge-pump control signal voltages in order to maximize the drive voltage range of the charge pump becomes an important requirement. That is, running high charge-pump currents with low-power supply voltages presents headroom challenges, particularly when considering process and temperature shift robustness[5,6].

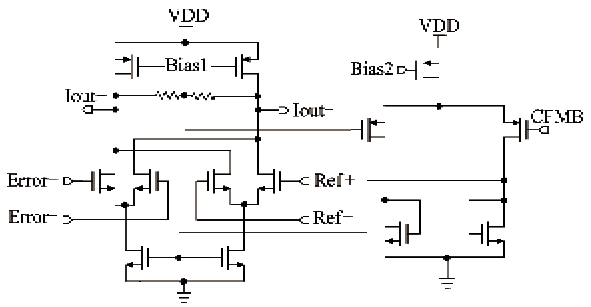

Fig. 6 The proposed differential charge pump

Proper differential operation is realized by the CMFB circuit, which also increases the output dynamic-range and the symmetry of charging or discharging current. In this work, the common-mode voltage of the charge pump outputs is sensed and compared to a common-mode reference CMFB.

3.3 LC-VCO

The simplified schematic diagram of the proposed complementary cross-coupling LC-VCO is shown in Fig. 7. The complementary structure features in oscillating more symmetry waveforms which results in the improvement of low-frequency flick noise. Moreover, the complementary structure produces a higher negative-resistor and as a result, a lower power dissipation. To suppress the common-mode noise introduced by power supply, substrate and control-line, a differential tuning technology is adopted. The frequency band of the proposed LC-VCO is extended up to 1.55Gb/s by employing switch capacitor array as shown in Fig. 8 and which is selectable by an external three-bit control word. For a low duty ratio distortion, a clock buffer with AC coupling is implemented. This buffer has a band-pass type transfer function, and so cuts off both low frequency noise caused by interference from the other surrounding circuits and high frequency harmonics generated in the LC-VCO[7]. The common-mode voltage of the output can be fixed by adjusting the bias.

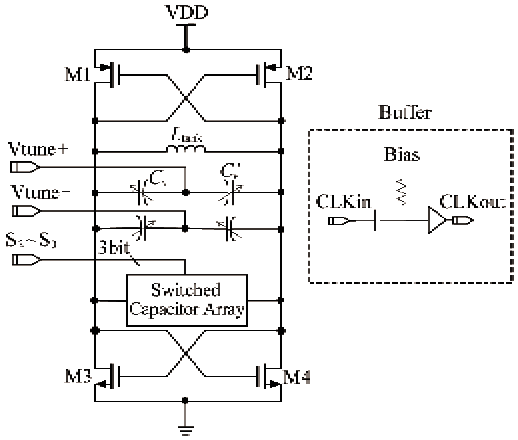

Fig. 7 Structure of LC-VCO and buffer

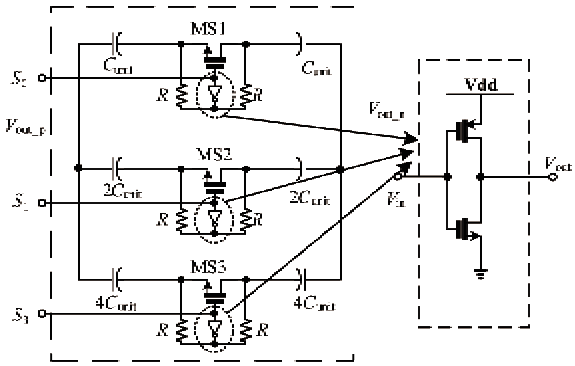

Fig. 8 The switch capacitor array of the VCO

The simulation results show that the VCO has a phase noise of −110dBc/Hz at 1MHz offset while consuming 5mA from a 1.0V supply. This phase noise performance will reduce the deterministic jitter of the recovered clock. However, it still brings a good random jitter characteristic that is acceptable for the 10Gb/s CDR operation[8].

3.4 Jitter attenuation PLL

An additional jitter attenuation PLL is used to meet jitter transfer specification, and it is a traditional second order PLL which bandwidth is set to be below 1MHz. In addition, considering the jitter peaking <0.1dB required by G.8251, the damping ratio should be designed to over-damped. The PFD and CP of the jitter attenuation PLL are carefully designed to avoid the dead zone of operation and to reduce mismatch of the system. The structure, tuning range and control word logic of the VCO are the same as the LC-VCO in the CDR PLL, excepting a single-ended "Vtune" as shown in Fig. 7.

4 Circuit simulation results

The transistor level circuits is simulated with

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Spectre@ RF simulator in the TSMC 65nm CMOS technology. The layout occupies an area of 0.975mm × 0.875mm as shown in Fig. 9 (including Pads for testing on-chip). The simulation results show that the VCO provides a tuning range of 2 GHz (≈19%) with a best phase noise of −110.7dBc/Hz at 1 MHz offset, and the maximum gain of the VCO is quite high, about 1.0GHz/V.

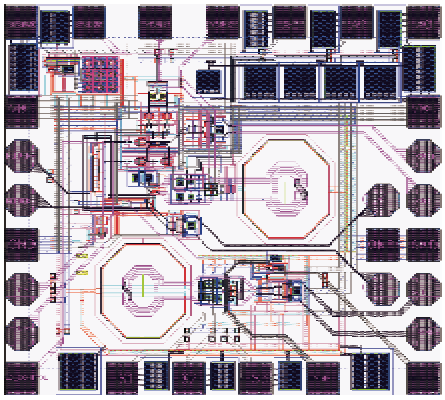

Fig. 9 Layout of the SerDes CDR

Fig. 10 shows an eye diagram of the recovery clock, exhibiting a peak to peak jitter of 5.17 ps. G.8251 specifies 0.1UI as the maximum peak-to-peak jitter on the recovery clock, and the measured jitter meets the requirements of G.8251.

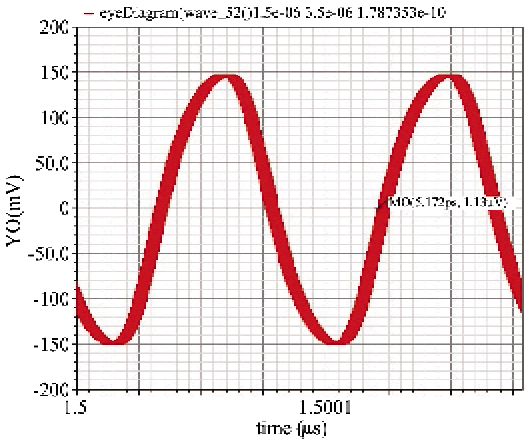

Fig. 10 Eye diagram of the recovery clock

Fig. 11 depicts the eye diagram of the recovered full-rate retimed date (11.2Gb/s). The retimed data exhibits a 280 mVpp output swing and a peak-to-peak jitter of 2.3ps. G.8251 specifies 0.15 unit interval as the maximum peak-to-peak jitter on recovered data, and the simulated results meet the requirements.

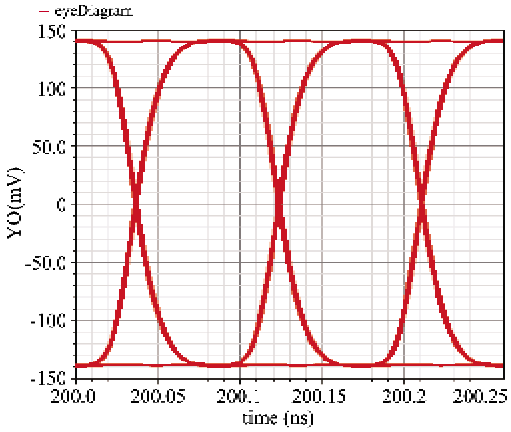

Fig. 11 Eye diagram of the recovery data (11.2Gb/s)

The simulated transient response of the differential control voltage of the CDR loop is shown in Fig. 12. Based on the mentioned design parameter, the locking time of the CDR can be less than 1.8μs by an initial frequency step.

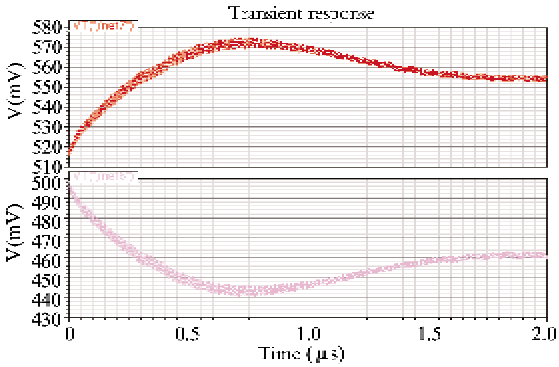

Fig. 12 The locking time of the CDR loop

5 Conclusion

This paper demonstrates a 9.95 ~ 11.5Gb/s CDR for SerDes application in 65nm CMOS technology. To conduct the whole CDR on the top level verification using standard digital simulator, the method for BLM in Verilog-HDL is innovated. A dual-loop architecture CDR PLL aided with jitter attenuation PLL is designed to simultaneously meet jitter tolerance and jitter transfer specifications defined in G.8251 of optical transport network (ITU-T OTN). The proposed oscillator, full-rate PD, differential charge pump and Flip-flop topologies resolve many of circuit and architecture issues. The jitter performance of the recovered clock and data preferably meet the jitter recommendations of G.8251.

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