doi:10.3772/j.issn.1006-6748.2014.03.016

A 14.5Gb/s word alignment circuit in 0.18μm CMOS technology for high-speed SerDes①

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Abstract

This paper presents a word alignment circuit for high speed SerDes system. By using pipeline structure and circuit optimization techniques, the speed of the aligner is increased, and its performance is improved further through adopting the full custom design method. The proposed word aligner has fabricated in 0.18μm CMOS technology with total area of $1.075 \times 0.775 mm^2$ including I/O pad. Measurement results show that this circuit achieves the maximum data rate of 14.5Gb/s, while consuming a total power of 34.9mW from a 1.8V supply.

Key words: comma detection, word alignment, pipeline, full custom, parallel structure

0 Introduction

SerDes[1,2], the abbreviation of the serializer/ deserializer, is a serial communication technology mainly used in the fiber system in the past. With the higher data throughput, lower power consumption and higher reliability, SerDes is replacing the traditional high-speed parallel bus interface technology which has become the bottleneck of further improving data transfer rate to become the mainstream interface mode. So it is very important to research SerDes system with high speed performance for promoting the development of communications industry.

The word alignment circuit, used in conjunction with the pattern detector to align the word boundary of the re-time data to a specified comma, is an important module in the SerDes receiver. It processes 10-bit parallel data coming from previous module DEMUX and has two main functions: comma detection and word alignment. The comma detection finds the signal "comma" which is usually used for frame synchronization, while the word alignment realizes the frame synchronization. It is very challenge to design a word alignment circuit for high speed SerDes using 0.18μm CMOS technology.

1 The structure of word alignment

The structure of word alignment can be classified into three types: (a) serial structure, (b) demultiplexer structure, and (c) parallel structure. The serial structure[3] is very simple, but has some disadvantages. For example, both comma detection and the word alignment module are on the serial path, making it hard to reduce the critical path delay and limiting the maximum working speed. In addition, dynamic power is much consumed due to the serial structure.

The second structure is composed of four parts[4]: a tree type 1:2 demultiplexer, a couple of serial type 1:5 demultiplexers, comma detector and a word alignment clock divider, shown as Fig. 1. Obviously, the power consumption is less than that of the first one. However, it also makes the critical path long and limits its working speed.

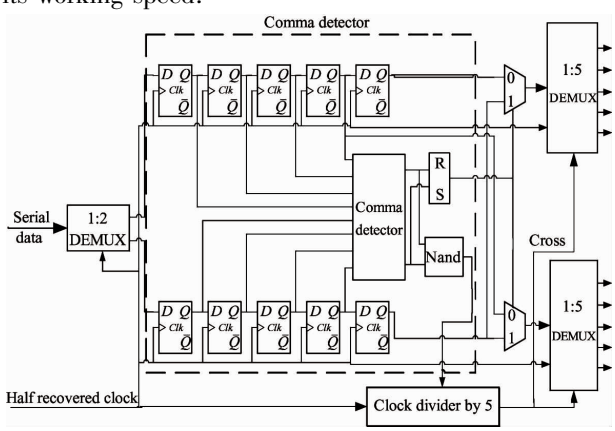

Fig. 1 Demultiplexer structure

The last structure is the parallel structure, which is shown as Fig. 2[5]. We can see that the comma detection and word alignment module are realized after

① Supported by the National High Technology Research and Development Programme of China (No. 2011AA10305).
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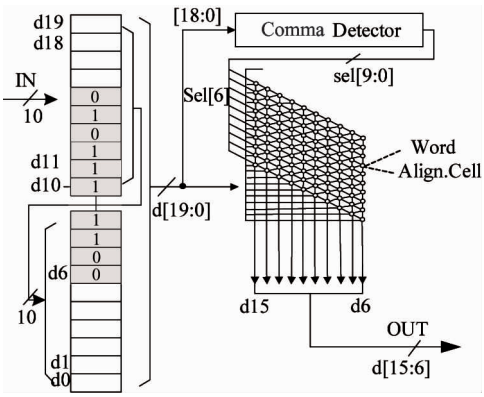
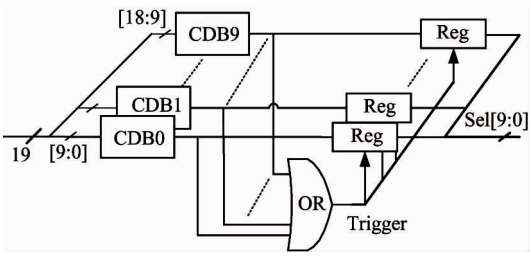
Received on May 29, 2013

the serial-parallel transformation in this structure. Therefore, the word aligner can work under lower clock frequency compared to the former two structures and can be implemented easily in 0.18μm CMOS technology. However, it is comprised of too many comma detection blocks (CDBs) and word alignment cells, which may increase the circuit delay. Moreover, the circuit is asynchronous and easier to be interfered by the jitters. Comparing the three structures, we choose the parallel structure as the major architecture, while optimizing and improving it for high performance.



(a) Block diagram of word alignment



(b) Comma detector module

Fig. 2 Parallel structure

2 High speed word alignment circuit

In this paper, a high speed word alignment circuit is realized by using synchronous and pipeline strategies. Fig. 3 is the block diagram of the proposed circuit mainly composed of the input buffer, CDBs, D Flip-Flops (DFFs), address latch, word alignment output network (WAON) and output buffer. *Datain*[9:0] and *Dataout*[9:0] are 10-bit input data and output data, respectively, while the output signal *comma* denotes that the word has been aligned. A group of DFFs is inserted between CDBs and address latch module with the purpose of increasing working speed of the whole circuit. Another advantage of the inserted DFFs is that it is helpful to the stability of the circuit. The control signal of address latch module is a registered signal "*trigger _ reg*".

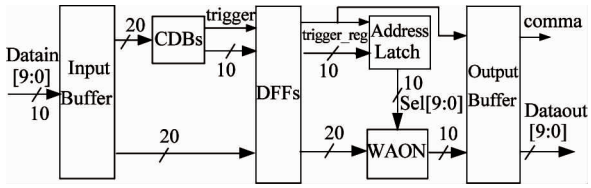


Fig. 3 Block diagram of the proposed structure

Next it will introduce how to further improve the speed and performance by optimizing the combinational logics and critical paths.

2.1 Optimization of CDBs and OR gate

Locating in the first stage pipeline, the CDBs are the important modules and very critical to the speed of whole circuit. Fig. 4 gives the block diagram of comma detection module, in which there are 10 CDB elements CDB0 ~ CDB9. The d0 ~ d9, d1 ~ d10, ⋯, d9 ~ d18 and DECT0 ~ DECT9 are their 10 inputs and outputs, respectively. The 10 outputs are then sent to an OR gate and its output acts as a trigger of the next module.

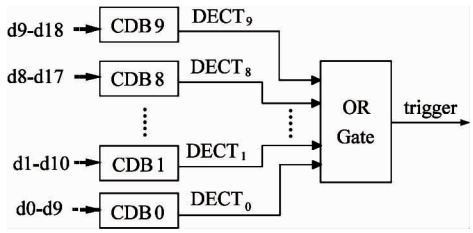


Fig. 4 Comma detection module

Below, it will take one of the combination logics CDB0 as an example to illustrate how to optimize CDBs. The output of CDB0 can be expressed as follows:

$$DECT_0 = \overline{d_0}\&\,\overline{d_1}\&d_2\&d_3\&d_4\&d_5\&d_6\&\,\overline{d_7}\&d_8\&\,\overline{d_9} \quad (1)$$

Then its corresponding schematic as shown in Fig. 5(a) is got. One can see that CDB0 consists of 21 basic gates such as NOT and NAND and there are 9 stages at most from input to output.

Eq. (2) indicates the simplification of Eq. (1), and the corresponding schematic is given in Fig. 5(b). It can be seen that the number of gates has been reduced from 21 to 17 and the maximum stage is only 5. Consequently, it is not difficult to verify that the delay of the optimized circuit is less than the original one.

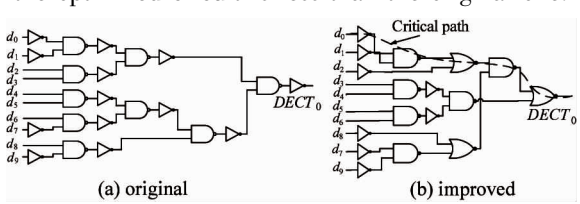


Fig. 5 CDB0 schematic

$$
\begin{aligned}
DECT_{0opt} &= \overline{\overline{DECT_0}} \\
&= \overline{\overline{d_0 \& \overline{d_1} \& d_2 \& \overline{d_7} \& \overline{d_9} \& d_8 \& d_3 \& d_4 \& d_5 \& d_6}} \\
&= \overline{\overline{d_0 \& \overline{d_1} \& d_2} \mid \overline{d_7 \& \overline{d_9} \& d_8} \mid \overline{d_3 \& d_4 \& d_5 \& d_6}} \\
&= \overline{(\overline{d_0 \& \overline{d_1}} \mid \overline{d_2}) \mid (\overline{d_7 \& \overline{d_9}} \mid \overline{d_8}) \mid \overline{(d_3 \& d_4) \& (d_5 \& d_6)}} \\
&= \overline{(\overline{d_0 \& \overline{d_1}} \mid \overline{d_2}) \mid (\overline{d_7 \& \overline{d_9}} \mid \overline{d_8}) \mid \overline{(d_3 \& d_4) \& (d_5 \& d_6)}} \\
&= \overline{\overline{d_0 \& \overline{d_1}} \mid \overline{d_2 \& \overline{d_7} \& \overline{d_9}} \mid \overline{d_8} \mid \overline{\overline{(d_3 \& d_4)} \& \overline{(d_5 \& d_6)}}}
\end{aligned}
\tag{2}
$$

To further optimize the delay of CDB0, the logic effort technique is used, in which each transistor in the critical path is designed elaborately to get the minimum delay. In Fig. 6, the critical path in CDB0 is rewritten to illustrate the timing optimization.

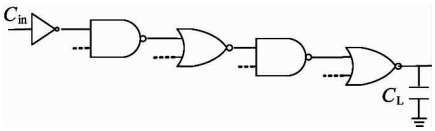


Fig. 6 The critical path in the CDB0 module

Assuming that g_i is the logical effort of the ith gate from left to right, C_{in} is the input capacitance of the first gate on the left, and C_L is the load capacitance of the last gate on the path, the total fanout F and total logic effort G can be expressed as follows.

$$F = \prod_{1}^{5} f_i = \frac{C_L}{C_{in}} \tag{3}$$

$$G = \prod_{1}^{5} g_i \tag{4}$$

Thus, the path effort $H = FG$. If each gate has the same effort $h = f_1 g_1 = f_2 g_2 = \ldots = f_5 g_5 = \sqrt[5]{H}$, then the minimum path delay can be obtained. Assuming that s_1 is the size of the first gate and there are no other branches, then the size of the ith gate is got as

$$s_i = \left(\frac{g_1 s_1}{g_i}\right) \prod_{j=1}^{i-1} f_i \tag{5}$$

Another large combination circuit needing to be considered is the 10-input OR gate. If the OR gate is designed in normal static CMOS logic as shown in Fig. 7(a), its area and delay will be large. Actually, in a clock cycle the comma signal appears only once in continuous 10 bits, that is to say, only one input among 10 inputs is "1" at most in one clock cycle. So, the OR gate can be made of the pseudo-NMOS circuit, shown as Fig. 7(b). It's easy to see that the number of transistors and delay are reduced significantly by using this structure.

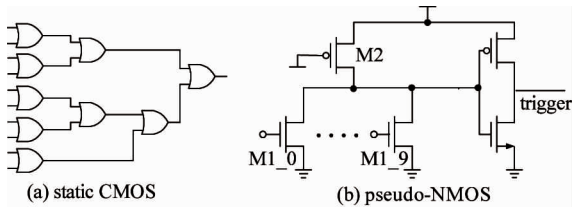


Fig. 7 The design of 10-input OR gate

2.2 TSPC-based DFF

DFF plays an important role in digital circuit, especially in timing optimization. It has been learned that the clock cycle is constrained by $t_{cycle} > t_{clk\text{-}Q} + t_{logic} + t_{setup}$, where $t_{clk\text{-}Q}$ and t_{setup} are all determined by DFF and t_{logic} is the delay of combination logics. To minimize the clock cycle, it optimizes the delay of DFF by employing high-speed DFF structure and full-custom design methodology. Particularly, a TSPC (true single phase clock) based DFF which is suitable for high speed operation is implemented in our design. Fig. 8 gives a typical TSPC DFF structure, in which the dynamic nodes are isolated by the static inverter[6]. The advantages of TSPC DFF include its high working speed, low power consumption, small area and single-phase clock control. TSPC DFF, however, has some drawbacks too. For example, it cannot work correctly when the edge of clock is slower since the slower clock change may make the clock-controlled NMOS and PMOS conduct simultaneously, resulting in incorrect state and competition.

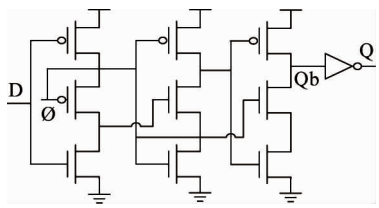


Fig. 8 the TSPC DFF

2.3 Word alignment output network

Once a comma signal is detected and a trigger signal is generated, the corresponding word boundary can be locked under the control of a registered trigger signal "*trigger_reg*". After that a 10-bit selecting signal is generated by the address latch module[7] and sent to WAON.

Fig. 9 is the structure of WAON, where *dataIn* and *dataOut* are 20-bit input and 10-bit output data, respectively and *sel*[9:0] is a 10-bit control signal which has only one '1' in a clock cycle at most. For example, if *sel*[9:0] is equal to "0000001000", meaning that *sel*[3] is '1' and all other bits are '0', then *dataIn*[12:3] is the output data.

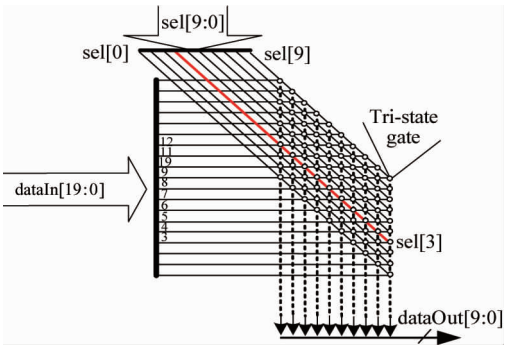


Fig. 9 Structure of WAON

The word alignment cell should be a tri-state gate because many cells are hooked to a bus. Fig. 10 gives three structures of tri-state gate, where the output is controlled by NOR gate, transmission gate, and NOT gate, respectively. The former two structures, in which output Y is connected to the dynamic gate whose input is X, have a common drawback that input X may affect the high level output voltage of Y due to the effect of charge sharing. The third structure, however, overcomes this issue and has another advantage that the enable signal EN on the critical path is very close to the output terminal, making the circuit performance better compared to the other structures. So the third structure is used in this paper.

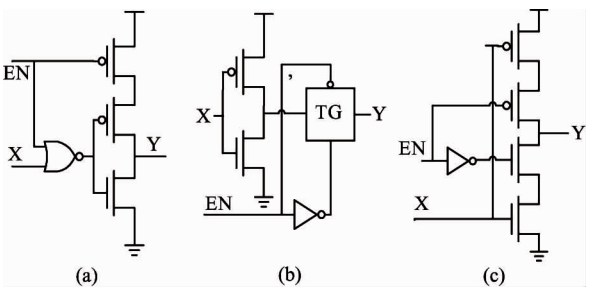


Fig. 10 Three structures of tri-state gate

3 Simulation and measurement results

The proposed word aligner has been designed and fabricated in TSMC 0.18μm CMOS technology. Fig. 11 shows the pre-simulation result with Spectral at SS corner, where the input data is a pseudo-random sequence including 10 different comma cases. When a comma signal appears in the parallel channels, the output signal trigger or CDB_{0-9} will become high indicating that "0011111010" has been detected. By comparing the output data with the original data, the function of the circuit can be simulated and verified. The pre-simulation results illustrate that the proposed circuit can work correctly at a data rate up to 15Gb/s.

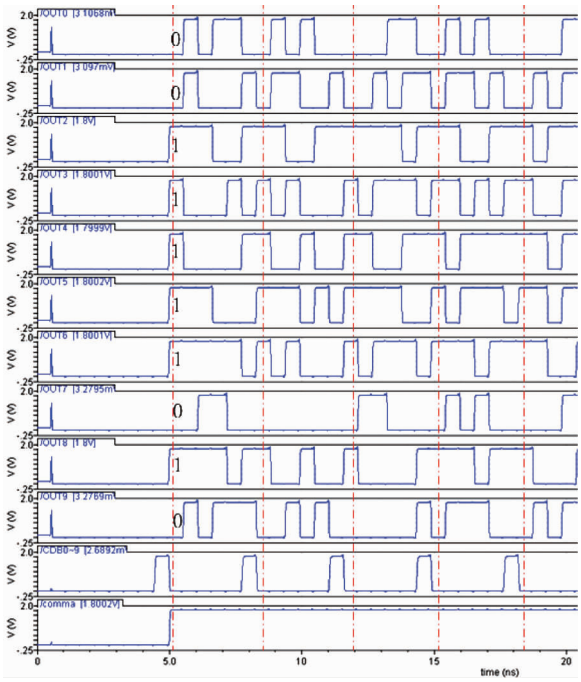


Fig. 11 Pre-simulation result at 15Gb/s

Fig. 12(a) is the layout of the core with an area of 0.375×0.275 mm^2 and Fig. 12(b) is the die photograph with a total area of 1.075×0.775mm^2 including I/O pad.

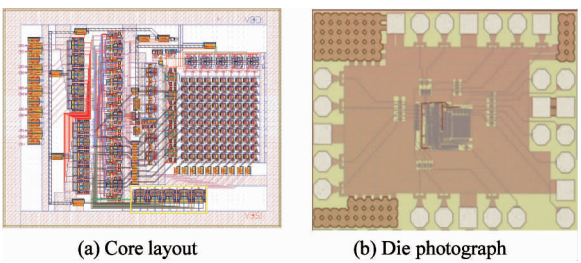


Fig. 12 Layout and chip photograph

Measurements are carried out on-wafer. All of the input signals are added from three sides except the right side, and the output signals are tested from the right side. Fig. 13 gives the measured results at the data rate of 14.5Gb/s, where Fig. 13(a) is the transient waveform of output signal *dataout*[0], *dataout*[2]

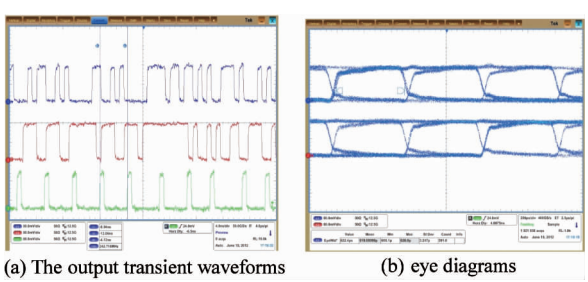


Fig. 13 Measured results at 14.5Gb/s

and *comma* from up to bottom, respectively, and Fig. 13(b) is the eye diagram of *dataout*[0] and *dataout*[2]. It is seen that the eye is open enough, illustrating that the word aligner can work correctly at a data rate of 14.5Gb/s. The measured power dissipation is 34.9mW at 14.5Gb/s with 1.8V power supply.

Table 1 displays the comparative result of these different design methods. Parameters of this design are listed in the last row of the table. It can be seen from the table that this design circuit's performance is far superior to the demultiplexer structure and better than the semi-custom parallel structure except area. The serial structure is not listed in Table 1 since its performance is far worse than that of the others'.

Table 1 Comparison of these designs

Architecture	Technology	Clock Speed	Chip Area	Power Consumption
demultiplexer structure	0.25μm	3.125Gb/s	1.3mm^2	234mW @3.3V
parallel structure (semi-custom)	0.18μm	6.25Gb/s	0.9mm^2	10.8mW @1.8V
parallel structure (full-custom)	0.18μm	14.5Gb/s	0.83mm^2	34.9mW @1.8V

4 Conclusions

A high speed and high stability word alignment circuit has been designed and fabricated in TSMC 0.18μm CMOS technology. By using the full custom design method and optimization techniques, its performance is improved significantly. The test result shows that the data rate can be up to 14.5Gb/s. This circuit can be used in high speed SerDes for 10 Gigabit Ethernet or SDH communication.

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