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Design of 5GHz low noise amplifier with HBM SiGe 0.13μm BiCMOS process①

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Abstract

A fully integrated low noise amplifier (LNA) for WLAN 802.11ac is presented in this article. A cascode topology combining BJT and MOS transistor is used for better performance. An inductive source degeneration is chosen to get 50Ohm impedance matching at the input. The noise contribution of common gate transistor is analyzed for the first time. The designed LNA is verified with IBM silicon-germanium (SiGe) 0.13μm BiCMOS process. The measured results show that the designed LNA has the gain of 13dB and NF of 2.8dB at the center frequency of 5.5GHz. The input reflection S11 and output reflection S22 are equal to −19dB and −11dB respectively. The P−1dB and IIP3 are −8.9dBm and 6.6dBm for the linearity performance respectively. The power consumption is only 1.3mW under the 1.2V supply. LNA achieves high gain, low noise, and high linearity performance, allowing it to be used for the WLAN 802.11ac applications.

Key words: low noise amplifier (LNA), noise figure (NF), WLAN802.11ac, S-parameters, SiGe BiCMOS

0 Introduction

The wireless local area network (WLAN) communication and home RF network are becoming popular as a part of our daily life. IEEE 802.11 is the first WLAN standard with data transmission rate of 2Mbps. To increase the data transmission rate, new generations of WLAN standards 802.11ac and HiperLAN/2 are defined which evolved from 2.4GHz to 5GHz spectrum. Compared with the 2.4GHz band, which is already heavily crowded, 802.11ac poses a significant advantage of using the relatively unused 5GHz band which is between 5.150GHz and 5.825GHz with a center frequency of 5.5GHz[1].

Low noise amplifier (LNA) is an important component in the RF front-end of WLAN802.11ac systems. It is the first block after an antenna and the noise performance of the whole system are mainly determined by it. In addition, other considerations also include the input impedance, maximum gain with sufficient linearity and a low power consumption[2-5].

The design of LNA in published reports mainly adopts the cascode topology to improve the Miller effects and isolation performance[6,7]. The common source and common gate stage in cascade topology always utilize the same type of MOS or BJT transistor. The process used is basically the CMOS, bipolar and BiCMOS. BiCMOS presents better performance because it combines the advantages of BJT and CMOS.

In this article, a design of fully integrated low noise amplifier with silicon-germanium (SiGe) IBM 0.13μm BiCMOS process for 802.11ac is presented. Section 1 discusses the detailed design of the proposed LNA including analysis of the input impedance and noise performance. The measurements result is in Section 2. Finally, Section 3 gives the conclusion.

1 Circuit design

Fig. 1 depicts the schematic of the proposed LNA. It is based on IBM 0.13μm SiGe BiCMOS technology which is an advanced process especially suitable for the wireless communications. The simulation is conducted in Cadence environment with circuit simulator SpectreRF.

A cascode topology is adopted in the design, which combines BJT and MOS transistor. The BJT transistor is used as the input transconductor due to its larger transconductance efficiency than that of MOS transistor. The common gate stage utilizes NMOS transistor which can provide small size for better reverse

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isolation. The cascode topology can improve the high frequency performance by the reduction of the Miller effect. In addition, it also provides a good isolation between output and input. An inductive source degeneration is chosen to create a real part of the input impedance without adding any resistor. The inductor that is used for biasing loading and output matching purposes, is used for both loading and matching the output of the circuit to 50Ω load impedance and also used for dc blocking of the output. The total node capacitance at the drain of resonates with inductance increases the gain at the center frequency and provides additional level of band-pass filtering simultaneously.

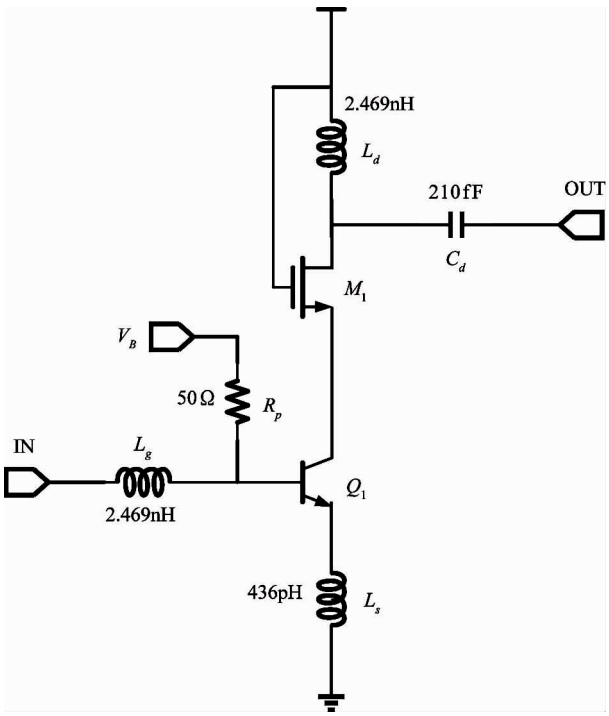

Fig. 1 The schematic of the proposed LNA

1.1 Input impedance matching

The quality of the input matching may greatly influence the overall performance of the design because the external antenna is typically connected by a transmission line with a characteristic impedance of 50Ω. The input impedance of LNA should be perfectly matched to 50Ω. The impedance matching guarantees maximum power-transfer and no reflections on the transmission line at the same time. The inductors L_g and L_s are used to achieve the impedance matching at the input. The impedance is derived based on the small signal equivalent circuit shown in Fig. 2 and equations should be satisfied at the frequency of interest, which is the design key of a single-band LNA's input impedance matching.

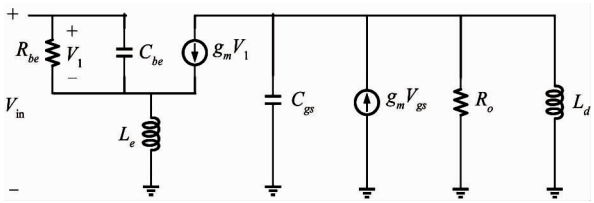

Fig. 2 Small signal equivalent circuit of the proposed LNA

The input impedance is

$$Z_{in} = (R_{be} // \frac{1}{sC_{be}}) + sL_e + \beta sL_e \quad (1)$$

Ignoring R_{be}, which is normally in hundreds of kilo Ohm range

$$Z_{in} = \frac{1}{sC_{be}} + sL_e + \beta sL_e \quad (2)$$

where

$$\beta = g_m \frac{V_1}{I_{in}} = \frac{g_m}{sC_{be}} \quad (3)$$

$$Z_{in} = \frac{1}{sC_{be}} + sL_e + \frac{g_m}{C_{be}} L_e \quad (4)$$

is got

The derivations above show that the source degeneration inductance increases the real part of the input impedance, providing us with convenience of matching at the operating frequency.

1.2 Noise analysis

The noise analysis is another key aspect in the design of LNA, which dominates the noise performance of the whole system because it is located at the 1st stage of the receiver. For a two-port amplification network as in Fig. 3, there is an equation for calculating the noise factor as follows[8].

$$F = 1 + \frac{\overline{v_n^2} + \overline{i_n^2} Z_S^2 + \overline{v_L^2} / |A_v|^2}{\overline{v_{ns}^2}} \quad (5)$$

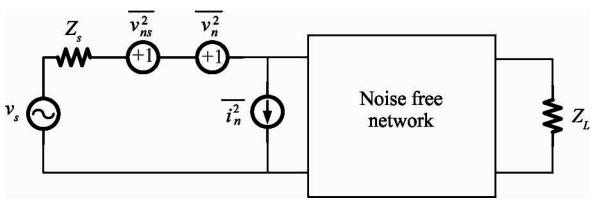

Fig. 3 General two-port network noise model

Fig. 4 gives the noise model of the proposed LNA. It includes a noise model of both common source BJT and common gate MOS transistor. While for the common gate (base) transistor, contributions of its noise is always ignored in previously published work. For the BJT noise model, BJT can be regarded as a two-port network, given as

$$F = 1 + \frac{r_b + r_e}{R_S} + \frac{1}{2}\frac{\omega_0}{\omega_T}Q + \frac{1}{2\beta Q}\frac{\omega_T}{\omega_0} + \frac{1}{2Q}\frac{\omega_0}{\omega_T} + \frac{\omega_0}{\omega_T}\frac{Q}{g_m R_C} \quad (6)$$

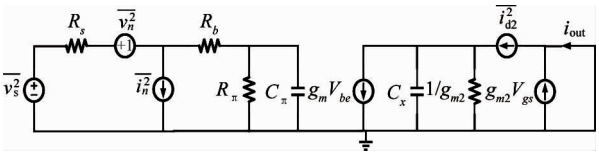

Fig. 4 Noise model of the proposed LNA

Then the influence of thermal noise of M1 channel is taken into considerations for the first time.

Supposing the transconductance expression of LNA:

$$G_m = \frac{g_m}{1 + j\omega_0 C_M R_S} \approx \frac{g_m}{j\omega_0 C_M R_S} \quad (7)$$

Converting the output noise current to the input noise voltage:

$$\overline{v_{in,d3}^2} = \frac{\overline{i_{out}^2}}{G_m^2} = 4kT\Delta f \gamma_3 g_{d0,3}\left(\frac{\omega_0 C_x}{g_{m3}}\right)^2\left(\frac{\omega_0 R_S}{\omega_T}\right)^2 \quad (8)$$

Therefore, the noise contribution of MOSFET is

$$\frac{\overline{v_{in,d3}^2}}{\overline{v_S^2}} = \gamma_3 g_{d0,3}\left(\frac{\omega_0 C_x}{g_{m3}}\right)^2\frac{\omega_0}{\omega_T}\frac{Q}{g_m} \quad (9)$$

here, C_x is the sum of junction capacitance and gate-source capacitance of MOS transistor and $g_{d0,3}$ is the conductance between the drain and the source under the zero bias condition. Therefore the noise factor of LNA considering the common gate NMOS transistor is

$$F = 1 + \frac{r_b + r_e}{R_S} + \frac{1}{2}\frac{\omega_0}{\omega_T}Q + \frac{1}{2\beta Q}\frac{\omega_T}{\omega_0} + \frac{1}{2Q}\frac{\omega_0}{\omega_T} + \frac{\omega_0}{\omega_T}\frac{Q}{g_m R_C} + \gamma_3 g_{d0,3}\left(\frac{\omega_0 C_x}{g_{m3}}\right)^2\frac{\omega_0}{\omega_T}\frac{Q}{g_m} \quad (10)$$

As the frequency is high enough, $\omega_0 C_x$ cannot be ignored anymore and the noise contribution from CG stage should be included. As a result, the channel thermal noise from common gate NMOS transistor also deteriorates the LNA noise figure and the above equation provides a design guidance of the NF optimization.

2 Measurement results

The prototype chip is fabricated with IBM silicon-germanium (SiGe) 0.13μm BiCMOS process. The photograph of chip is shown in Fig. 5. The chip area is 700μm × 500μm and the current consumption is about 1.1mA with 1.2V supply voltage. The chip is tested via on-wafer probing. The measurements are carried out with an Agilent E4438C vector network analyzer and an E4440A spectrum analyzer.

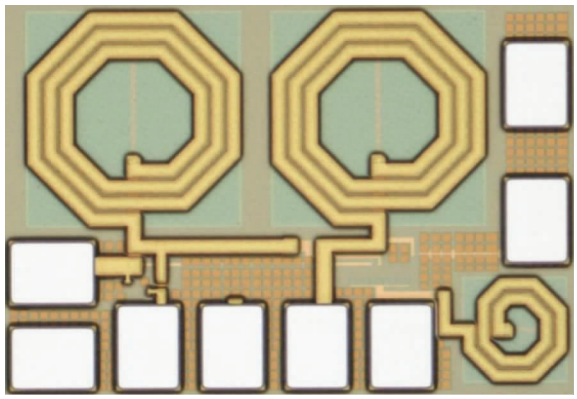

Fig. 5 Die photograph

In Fig. 6, it can be seen that measured S_{21} is 13dB at the center frequency of 5.5GHz and −3dB bandwidth is 500MHz. Fig. 7 gives S_{11}, S_{22}, S_{12} which are −18dB, −12dB and −26dB respectively.

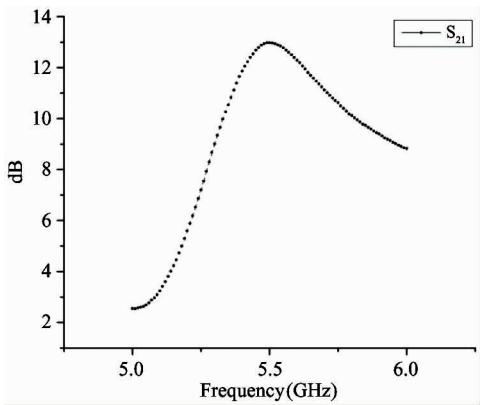

Fig. 6 Measured S_{21}

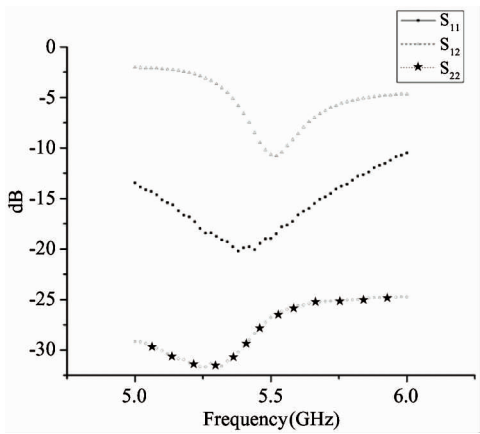

Fig. 7 Measured S_{11}, S_{22} and S_{12}

Fig. 8 shows NF of LNA. NF at 5.5GHz center frequency point is 2.8dB. The NF value within the 5.1 – 5.8GHz bandwidth is below 3.1dBm and the minimum NF is located at 5.2GHz. As Fig. 9 shows, LNA exhibits an 8.9dBm of input P – 1dB and a 6.6dBm of IIP3. The proposed LNA meets well the requirements in IEEE802.11ac WLAN applications.

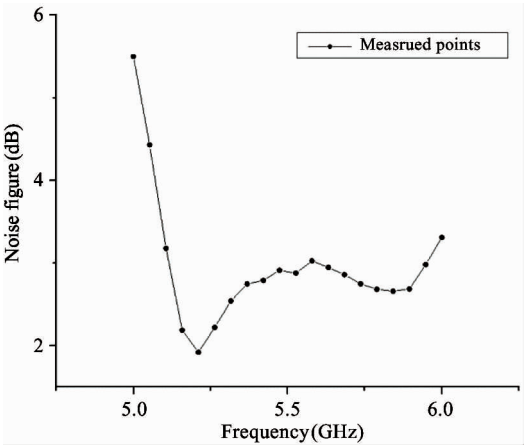

Fig. 8 Noise figure

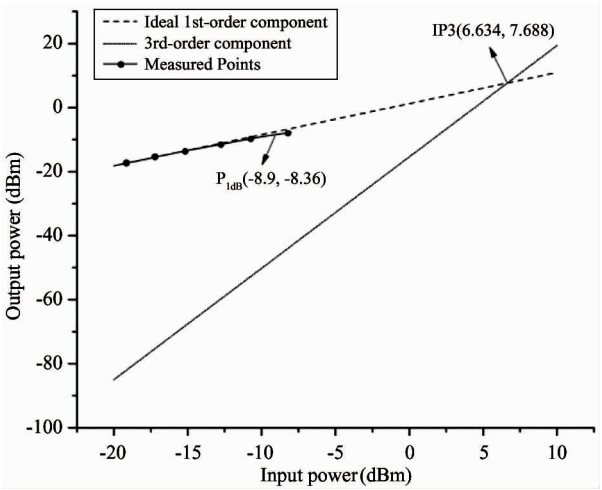

Fig. 9 Measured IIP3

To compare the LNA performance with the other published work, the Figure of Merit (FoM) which takes account of the gain, NF and power consumption is considered. Table 1 gives the performance summary and the comparison. From the table, it can be seen that our work achieves the highest FoM.

Table 1 Performance summary of the LNA

Reference	This work	Ref. [9]	Ref. [10]	Ref. [11]	Ref. [12]	Ref. [13]	Ref. [14]
Frequency (GHz)	5.5	1 – 5.2	3 – 10	5.15 – 5.825	5 – 6	3 – 10	0.5 – 8.2
Gain(dB)	13	17	21	15.7	15	17	25
NF(dB)	2.8	2.5	2.5 – 4.2	2.23	2.75	3.5 – 4.3	1.9 – 2.6
IIP3(dBm)	8.4	–	– 5.5	–	–	–	–
Reverse isolation (dB)	32	–	–	–	–	–	–
Power(mW)	1.3	18	30	24.8	10.6	14.4	42
Process	130nm SiGe	180nm SiGe	180nm SiGe	250nm SiGe	350nm CMOS	65nm CMOS	90nm CMOS
Area(mm^2)	0.35	0.3	–	0.69	0.55	0.15	0.025
FoM	16.95	2.84	3.68	2.21	3.38	2.39	11.4

$$\mathrm{FoM}[\mathrm{mW}^{-1}] = \frac{\mathrm{Gain}[\mathrm{abs}]}{(\mathrm{NF}-1)[\mathrm{abs}]\,P_{DC}[\mathrm{mW}]} \quad (11)$$

Good performance is due to the following two aspects. As analyzed in Section 2, combination of MOS and BJT improves the frequency performance. Although the noise performance of the MOS transistor is less than that of the BJT transistor because of the 1/f noise, but for the common gate device, contribution of CG MOSFET on the overall noise is acceptable. In addition, the IBM 0.13μm SiGe BiCMOS process is suitable for the RF design that works in the low supply and low current consumptions.

3 Conclusions

A fully integrated low noise amplifier with IBM silicon-germanium (SiGe) 0.13μm BiCMOS process for WLAN 802.11ac is presented in this article. It uses the cascode topology combining mixed MOS and bipolar transistor to improve the reverse isolation. The measured results show that the designed LNA provides high gain, low noise, and high linearity performance with only 1.3mW power consumption. It meets well the requirements in WLAN 802.11ac applications.

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