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# A fractional frequency divider based on phase switching and negative feedback delta-sigma modulator for MMMS applications①

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**Abstract**

A fractional frequency divider based on phase switching and negative feedback delta-sigma modulator (NF-DSM) is presented. The phase switching circuit, realized by switching 8 signals generated by a divider-by-4 circuit, is adopted to reduce the frequency division step. The NF-DSM, which can obtain smooth output spectra, is proposed to generate the fractional part of the division ratio, moreover, the integer part of the division ratio is realized by a divider-by-2/3 circuit chain. Fabricated in TSMC 0.18 μm RF CMOS technology, the fractional frequency divider achieves a measured operation frequency from 0.5 GHz to 8 GHz. With a 1.8 V supply voltage, the maximum current consumption of the whole divider is 17.5 mA, and the chip area is 0.58 $mm^2$, including the pads.

**Key words**: delta-sigma modulator(DSM), divider-by-2/3, frequency divider, phase switching

## 0 Introduction

As the rapid development of various wireless communication standards, there is a strong trend in integrating all transceiver circuits, which support the multi-mode and multi-standard (MMMS) communication systems in a single chip. Therefore, the multi-mode multi-frequency (MMMF) broadband frequency synthesizer [1-3], which is indispensable in a multi-mode RF (radio frequency) transceiver, has become a research hot spot recently.

Typically, a fractional frequency synthesizer is constituted by phase-frequency detector (PFD), current pump (CP), loop filter (LF), voltage-controlled oscillator (VCO), and fractional frequency divider chain. Furthermore, the fractional frequency divider chain consists of the programmable frequency divider and delta-sigma modulator. The programmable frequency divider, as a critical module in MMMF frequency synthesizers, is required to work under a broad and high frequency range[4,5]. Due to the low highest working frequency[6,7], the traditional programmable divider based on flip-flops and combinational logic circuits is not able to meet the requirements of the MMMF frequency synthesizers. But the programmable frequency divider based on phase switching can not only operate in a higher frequency, but also can achieve a 0.5 decimal frequency division step, which is conducive to suppress the quantization noise of the modulator[8]. Hence, a phase-switching circuit based on a divider-by-4 circuit is presented.

Moreover, the delta-sigma modulator (DSM) is also widely used in the fractional frequency divider to generate fractional division ratio. For the traditional DSM, since its output sequence length is affected heavily by input values and initial conditions[9,10], when the input values and/or initial conditions are set inappropriately, its output sequence length may become very short, which causes obvious high-power spurious tones in the output spectrum of the frequency synthesizer. Thus, a negative feedback delta-sigma modulator (NF-DSM) that can obtain spur-free output spectra is proposed.

Therefore, the fractional frequency divider based on the phase switching and negative feedback delta-sigma modulator is presented in this paper. The rest of the paper is organized as follows. In Section 1, an architecture of the fractional frequency divider is described briefly. Then, Section 2 gives the detailed circuits design of each block. Next, the measured results are presented in Section 3. Finally, Section 4 concludes the whole work.

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## 1 Architecture of the fractional frequency divider

The architecture of the fractional frequency divider is shown in Fig. 1, which is composed of three main parts. The first part is a high-speed divider-by-2 circuit, which is used to generate the quadrature I/Q output signals and lower the output frequency of the VCO. The second part is a 0.5 step programmable frequency divider based on a phase switching logic. The frequency division ratio of the phase switching circuit ranges from 0.5 to 4 with 0.5 step size, and the divider-by-2/3 chain broadens the frequency division ratio range further. The last part is a delta-sigma modulator with negative feedback, which is used to generate the control word for the fractional division ratio.

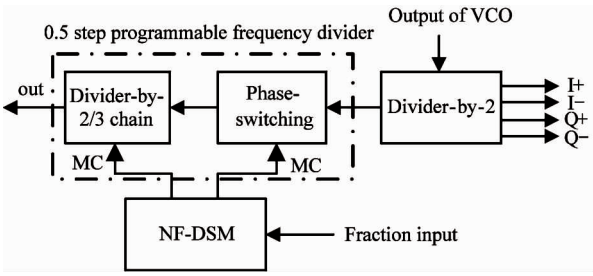



**Fig. 1** Architecture of the fractional frequency divider

## 2 Circuit design

### 2.1 Divider-by-2 circuit

Due to the high operating frequency, the divider-by-2 circuit is implemented by the current mode logic (CML) circuit. As shown in Fig. 2, the divider-by-2 circuit is composed of a CML flip-flop, which is made up of two CML latches. The CML latch comprises a sampling stage and a latch stage. Thereinto, the sampling stage is composed of $M1$ and $M2$, and the cross coupling transistors $M3$ and $M4$ form the latch stage. In addition, the maximum operating frequency can be enhanced further by the inductor load, and the parallel peaking technique can be also used to improve the bandwidth of the CML latch[11]. The tail current source is used to provide a DC operating point to limit power consumption. However, if a higher speed or lower voltage is required, the tail current source can be removed.

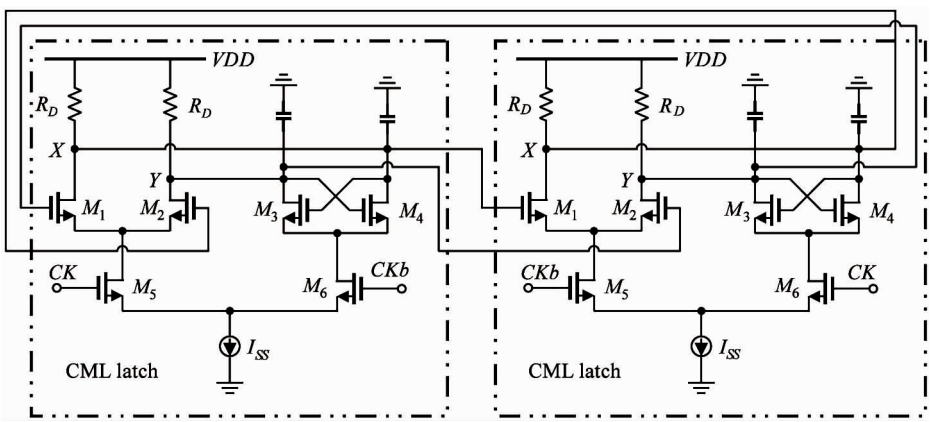



**Fig. 2** Schematic of the divider-by-2 circuit

The working principle of the CML latch is as follows. When $CK$ is high, $M5$ turns on while $M6$ turns off, the latch is in the sampling state, $M1$ and $M2$ sample the input signal, and the output is amplified. When $CK$ becomes low, $M5$ turns off and $M6$ turns on, which make the CML latch enter into the latch state, i.e. $M1$ and $M2$ stop working in this case, and the cross coupling transistors $M3$ and $M4$ form a positive feedback to latch the output signal. The peak to peak amplitude of the output signal is $I_{SS}R_D$ when the bandwidth is not restricted, where $I_{SS}$ is the tail current source, $R_D$ is the load resistance.

### 2.2 Phase switching circuit

The phase switching circuit is composed of a divider-by-4 circuit, an analog multiplexer and a logic control circuit, as shown in Fig. 3. First, the input signal is divided by the divider-by-4 circuit to generate the eight-phase clock signals with 45-degree phase difference between each other. Under the control of logic control circuit, the analog multiplexer switches among the eight signals to select a clock as the output at each moment. Thus, different frequency ratio ranging from 0.5 to 4 with a step of 0.5 can be achieved

by controlling the logic control circuit. Note that, the phase-switching circuit needs to be able to switch freely in the eight frequency division ratios.

The divider-by-4 circuit consists of four CML latches, which are the same as the latches used in the divider-by-2 circuit. Usually, the divider-by-2 circuit, which is less complicated than the divide-by-4 circuit, can be used to generate four phase-switching signals. However, compared with the divider-by-2 circuit, the divider-by-4 circuit can further reduce the input frequency, which improves the stability of the phase-switching waveforms and lowers the power consumption, since the operation frequency is much lower and the transistors usually work in the switch state.

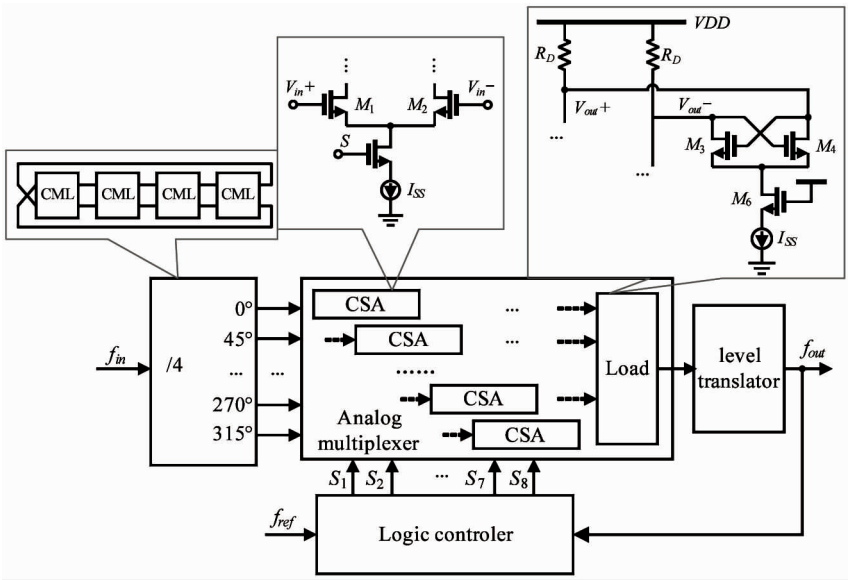



**Fig. 3** Structure of the phase switching circuit

Next, connecting eight parallel differential common source amplifiers (CSAs) constructs the analog multiplexer. In order to ensure that only one CSA is working at each time instant, the tail current source of each CSA is controlled by a switch. The cross coupling transistors are used in the analog multiplexer to reduce the transition time of the output signal. Note that, in order to avoid large transmission delay, the size of the cross coupling transistors cannot be too large. Finally, the forward switching method[5,8] is chosen to avoid the glitch in the phase-switching process, and the logic control circuit is carefully designed to ensure the correct switching mode and switching times.

## 2.3 Integer programmable frequency divider

The integer programmable frequency divider is realized by 2/3 divider chain[12], which has many advantages. For example, each module of the 2/3 divider chain is reusable and can be optimized individually, which simplifies the circuit design in some extent. Moreover, it can reduce the working frequency of the whole circuit step by step, which lowers the power consumption of each module exponentially. As shown in Fig. 4, the integer programmable frequency divider is constituted by six cascaded 2/3 dividers and a combinational logic circuit. The combinational logic circuit is used to expand the frequency division ratio further. It works as follows.

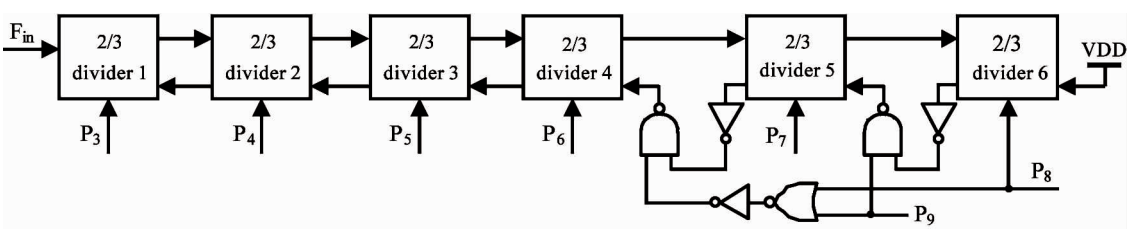



**Fig. 4** Structure of the integer programmable frequency divider

When $P_9$ is logic '1', since the combinational logic circuit does not affect the work of the frequency divider, all the 2/3 dividers are working. In this case, the minimum and maximum frequency division ratios

are 64 and 127, respectively. When $P_9$ is logic '0', the sixth 2/3 divider is turned off, thus, the minimum and maximum frequency division ratios are 32 and 63, respectively. When $P_8$ and $P_9$ are both logic '0', only the first four 2/3 dividers are working, hence, the minimum and maximum frequency division ratios are 16 and 31, respectively. Consequently, the 2/3 divider chain covers the frequency division ratio ranging from 16 to 127. Moreover, we should note that, an extra combinational logic circuit is also needed to choose the appropriate 2/3 divider as the output, which is not presented in Fig. 4.

From Fig. 5, it is known the 2/3 divider consists of four latches and three AND gates. The principle of the 2/3 divider is as follows. When P and $\mathrm{mod}_i$ is logic '1', latch 1 and 2, latch 3 and 4 form two D flip-flops respectively. So the 2/3 divider performs divider-by-3. While if P or $\mathrm{mod}_i$ is logic '0', the output of latch 3 is always logic '1' and the latches form a D flip-flop, then the 2/3 divider performs divider-by-2. The schematic of the 2/3 divider realized by TSPC logic is shown in Fig. 6.

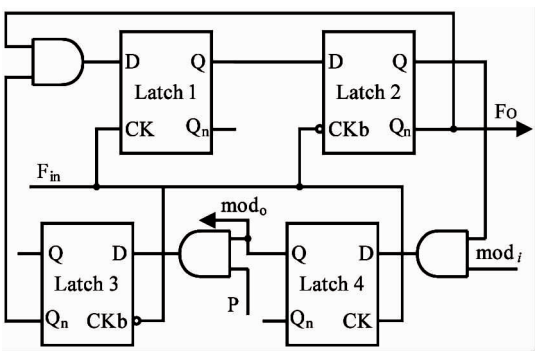



**Fig. 5** Structure of the 2/3 divider

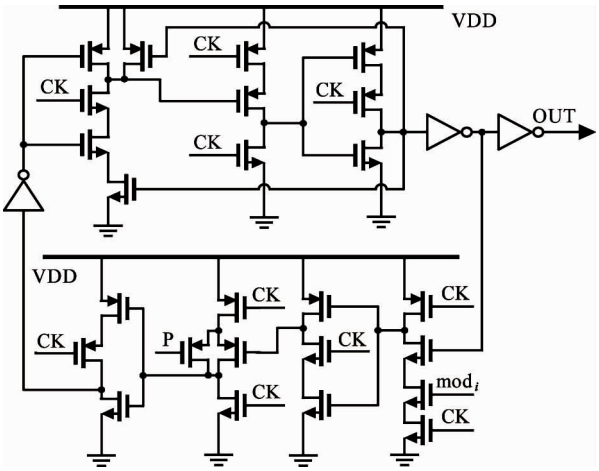



**Fig. 6** Schematic of the TSPC 2/3 divider

## 2.4 Negative feedback delta-sigma modulator

Fig. 7 shows the block diagram of the traditional $l^{\mathrm{th}}$-order multi-stage noise shaping (MASH) delta-sigma modulator, which is constructed by $l$ first-order error feedback modulator (EFM) stages and an error cancellation logic (ECL) network. For the traditional MASH DSM, since its output sequence length is affected by the input values and initial conditions heavily, when these conditions are set inappropriately, its output appears obvious tonal spectrum[9,10]. Fig. 8(a) and (b) show the influence of the input values and initial conditions on the output spectrum of the third-order MASH 1-1-1 DSM, respectively, with wordlength $n_0 = 14$. In Fig. 8(a), the inputs are $X = 2^{13}$ and $X = 2^{13} + 1$, respectively, with the initial conditions $S_1[0]S_2[0]S_3[0] = 000$. As can be seen, when the input is $X = 2^{13}$, the output has only two spurious tones, without noise shaping. While when the input is $X = 2^{13} + 1$, the output spectrum is smooth relatively and the noise

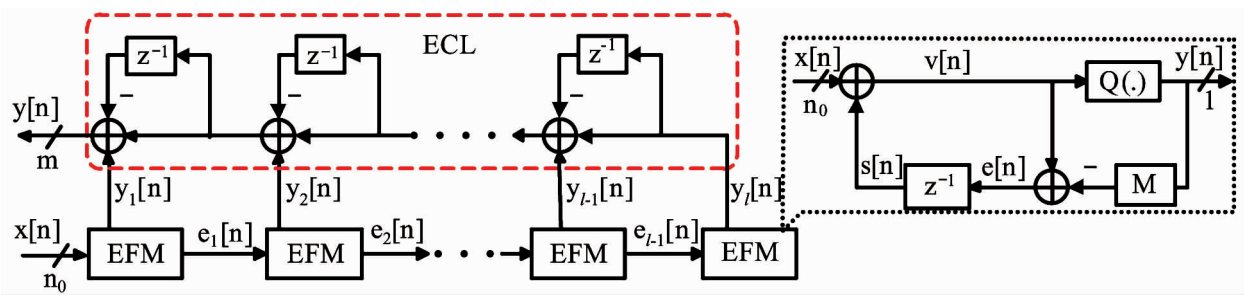
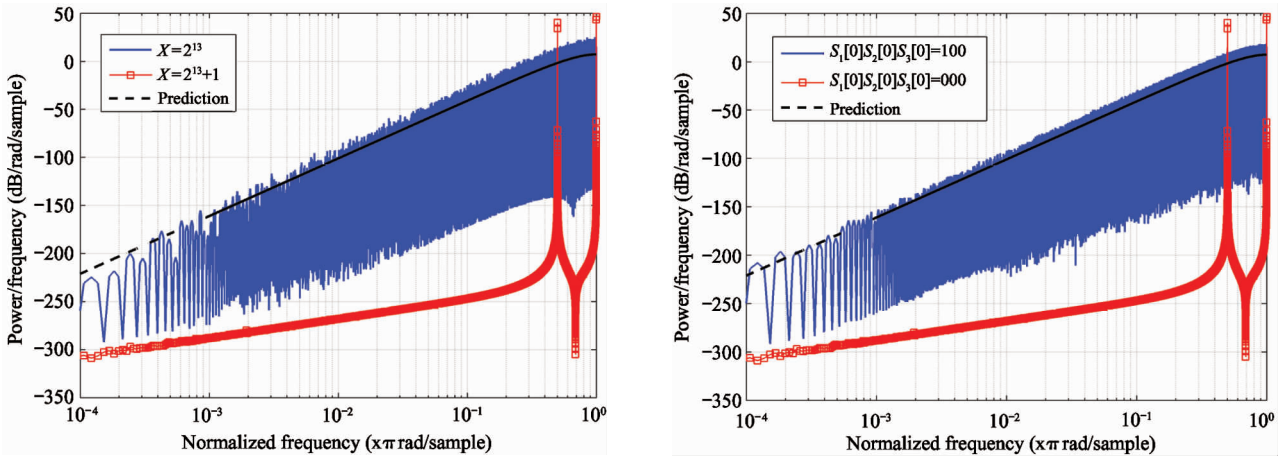



**Fig. 7** Block diagram of the traditional $l^{\mathrm{th}}$-order MASH DSM

is shaped well. In Fig. 8(b), the initial conditions are $S_1[0]S_2[0]S_3[0] = 000$ and $S_1[0]S_2[0]S_3[0] = 100$, respectively, with the input $X = 2^{13}$. See that, when the initial conditions change from '000' to '100', the output spectrum also changes from the spurious tones to the smooth spectrum.

Thus, in order to obtain a smooth output spectrum, many techniques have been proposed to extend the output sequence length, such as adding the additive dither signal into the DSM[9,10], and modifying the architecture of the DSM[13,14].




(a) $X=2^{13}$ and $X=2^{13}+1$, with $S_1[0]S_2[0]S_3[0]=000$ (b) $S_1[0]S_2[0]S_3[0]=000$ and $S_1[0]S_2[0]S_3[0]=100$, with $X=2^{13}$

**Fig. 8** Simulated output spectra of the third-order MASH 1-1-1 DSM

A negative feedback DSM (NF-DSM) is proposed to obtain the smooth output spectra for all the allowed inputs and initial conditions. As shown in Fig. 9, an extra negative feedback block $bz^{-1}$ between the output and the input is added, where $b$ is a carefully-chosen positive integer to make $(M+b)$ the smallest prime number above $M(M=2^n)$. For convenience, the values of $b$ for different input wordlength $n$ are summarized in Table 1. In the $z$-domain, for the first stage, its input includes the negative feedback signal from the output and the constant input signal, so, its output can be written as

$$Y_1(z)=\frac{X(z)-bz^{-1}Y(z)}{M}-\frac{E_1(z)}{M}(1-z^{-1}) \tag{1}$$

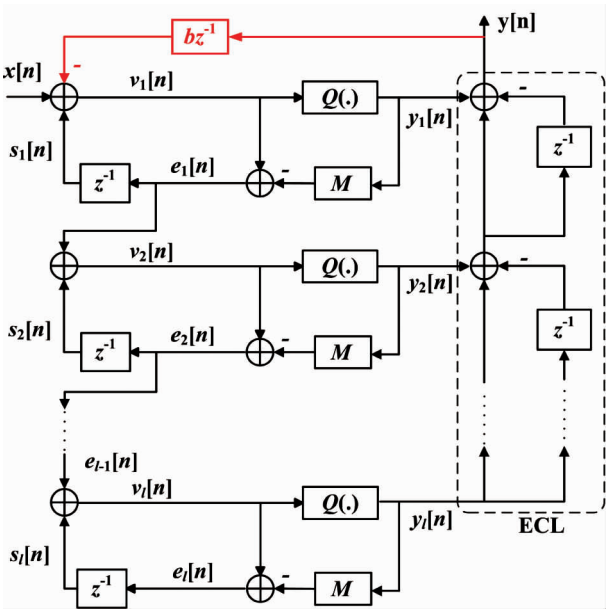



**Fig. 9** Block diagram of the negative MASH DSM

Table 1 Corresponding values of $b$ with respect to the input wordlength $n$ varying from 6 to 30

| $n$ | $b$ |
|---|---|
| 8, 16 | 1 |
| 6, 7, 12, 15, 18, 28, 30 | 3 |
| 11 | 5 |
| 10, 20 | 7 |
| 9, 23 | 9 |
| 29 | 11 |
| 22, 26 | 15 |
| 13, 21 | 17 |
| 19 | 21 |
| 14 | 27 |
| 17, 27 | 29 |
| 25 | 35 |
| 24 | 43 |

Then, for the rest stages, since the input of each stage is the quantization error of the previous stage, the outputs can be expressed as

$$Y_2(z)=\frac{E_1(z)}{M}-\frac{E_2(z)}{M}(1-z^{-1}) \tag{2}$$

…

$$Y_l(z)=\frac{E_{l-1}(z)}{M}-\frac{E_l(z)}{M}(1-z^{-1}) \tag{3}$$

Next, observing the ECL circuit, there is

$$Y(z)=Y_1(z)+Y_2(z)(1-z^{-1})+\cdots+Y_l(z)(1-z^{-1})^{l-1} \tag{4}$$

Finally, substituting Eqs(1), (2), and (3) into Eq. (4), the output of the NF-DSM is got:

$$Y(z)=\frac{X(z)}{M+bz^{-1}}-\frac{E_l(z)}{M+bz^{-1}}(1-z^{-1})^l \tag{5}$$

Moreover, it is also noted that, the negative feedback limits the input range of the NF-DSM in some extent. For example, for the third-order MASH 1-1-1

NF-DSM, its output is in the range of $-3$ to 4 [15]. Hence, in order to avoid the overflow in the input port, one should make sure that the input satisfies:

$$4b \leqslant X < M - 3b \tag{6}$$

For example, when the wordlength $n=6$, negative feedback factor $b=3$, the input range should be $12 \leqslant X < 55$. The simulated output spectra of all the allowed inputs are shown in Fig. 10, with the initial condition $S_1[0]S_2[0]S_3[0]=000$. As can be seen, in all the cases, the output spectra are smooth and the quantization noise is shaped well.

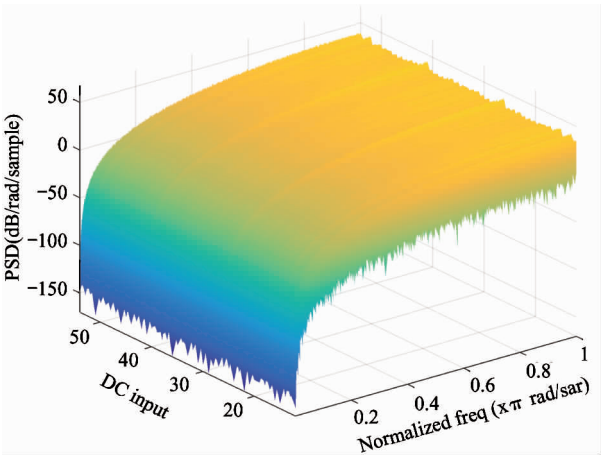



**Fig. 10** Simulated output spectra of the third-order MASH 1-1-1 NF-DSM for all the allowed inputs with $n=6$, $b=3$, and $S_1[0]S_2[0]S_3[0]=000$

Thus, based on the above analysis, in the fractional frequency divider, a 20-bit MASH 1-1-1 NF-DSM with $b=7$ is designed, to obtain the fractional division ratio. Since it is difficult to test the output spectrum of the NF-DSM in the fractional frequency divider directly, the 20-bit MASH 1-1-1 NF-DSM with $b=7$ is implemented on an Altera Cyclone II FPGA with an Analog Device AD9708 DAC board. An Agilent E4440A spectrum analyzer is used to measure the output spectrum. With input $X=2^{19}$, the experimentally measured output spectrum of the modulator is presented in Fig. 11. As can be seen, the measured output spectrum is smooth and spur-free over the entire frequency range, which is consistent with the simulations.

## 3 Measured results

The fractional frequency divider is implemented in TSMC 0.18 μm RF CMOS process. The microphotograph of the chip is shown in Fig. 12. The die area is 0.58 $mm^2$, including pads. The whole circuit (including testing buffers) draws 14.34 mA and 17.5 mA from 1.8 V supply when the input frequencies are 0.5 GHz and 8 GHz respectively.

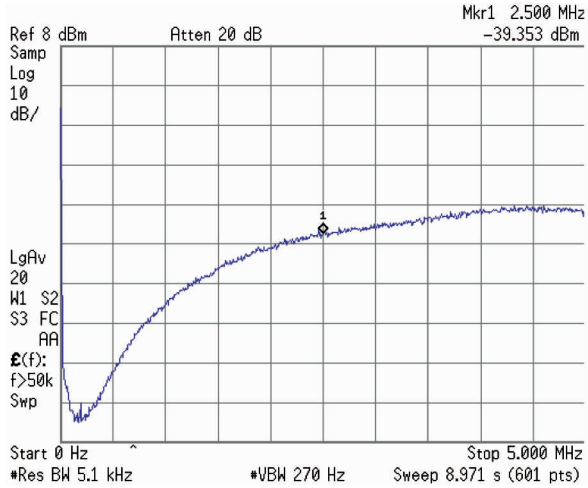



**Fig. 11** Measured output spectra of a 20-bit SNF-MASH 1-1-1 with input $X=2^{19}$

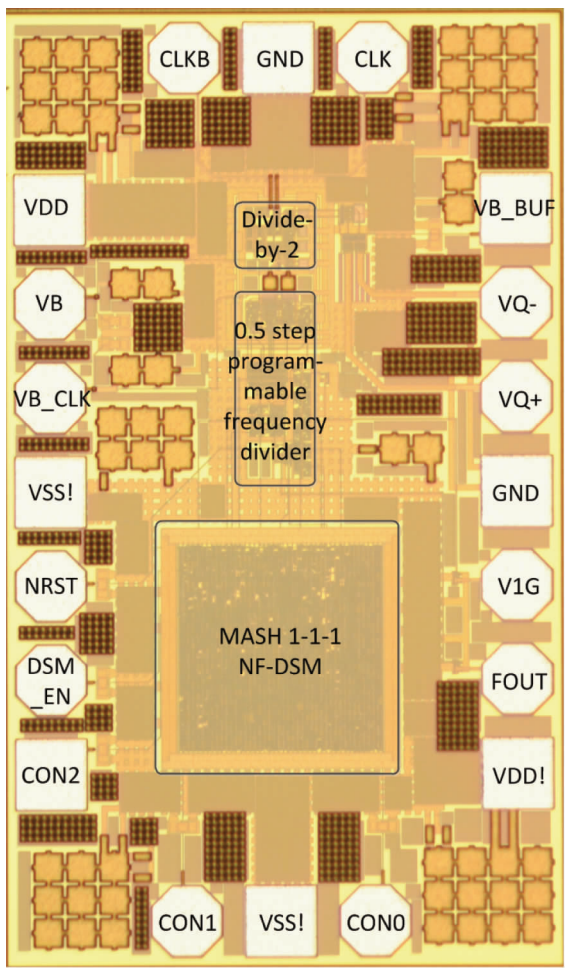



**Fig. 12** Microphotograph of the chip

First, turning on the divider-by-2 circuit only, and its self-resonant spectrum is measured, as shown in Fig. 13 that the divider-by-2 circuit oscillates at about 3 GHz. From which, it can be predicted that the most sensitive input frequency of the divider-by-2 cir-

cuit is about 6 GHz. In order to verify this prediction, Fig. 14 presents the input sensitivity curves of the divider-by-2 circuit measured by three different chips, i. e. chip1, chip2, and chip3, with the rest circuits turned off. Moreover, the curve of chip3 _ 1 is measured by chip3 under the condition that the rest circuit blocks are working. As can be seen, when the input frequency is about 6 GHz, the required input power is minimum in all the four cases, as predicted. Finally, from the curve chip3 _ 1 one can find that, when the rest digital circuits are in working state, the input sensitivity of the divider-by-2 is reduced, which means the digital circuits interfere the working of divider-by-2 circuit in some extent.

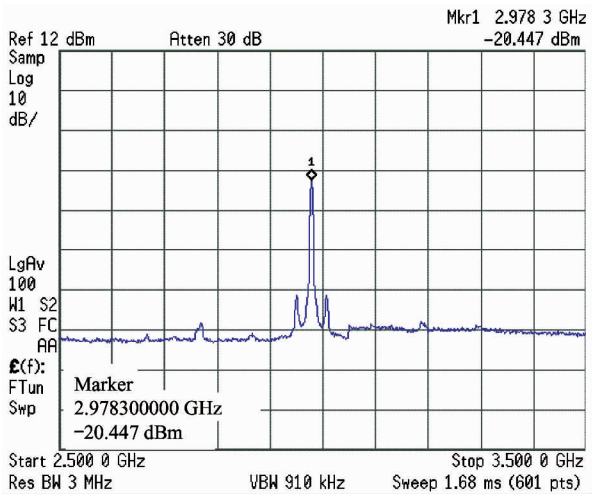



**Fig. 13** Self-resonant spectrum of the divider-by-2 circuit

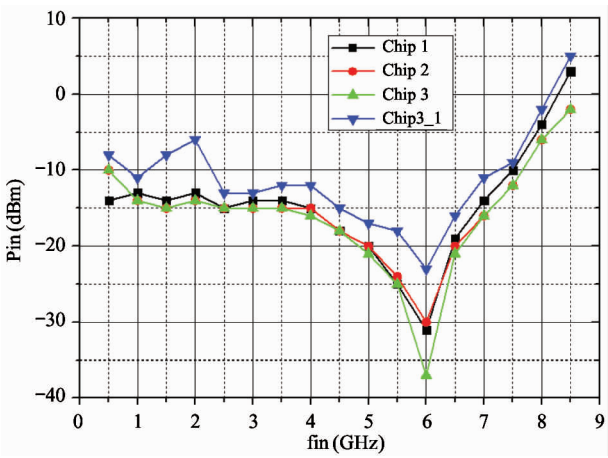



**Fig. 14** Input sensitivity curve of the divider-by-2 circuit

Next, turning on the whole fractional frequency divider and setting the input frequency as 0.5 GHz and the division ratio as 129.125, the output spectrum is measured, as presented in Fig. 15. It shows that the divided output frequency is about 3.878 MHz, as predicted. Moreover, Fig. 16 shows the measured output spectrum when the input frequency is 8 GHz and the division ratio is 1008.875. As can be seen, the output frequency is about 7.927 MHz, which is also correct within a reasonable error range. The measured results show that, the fractional frequency divider can work correctly with input frequency varying from 0.5 GHz to 8 GHz.

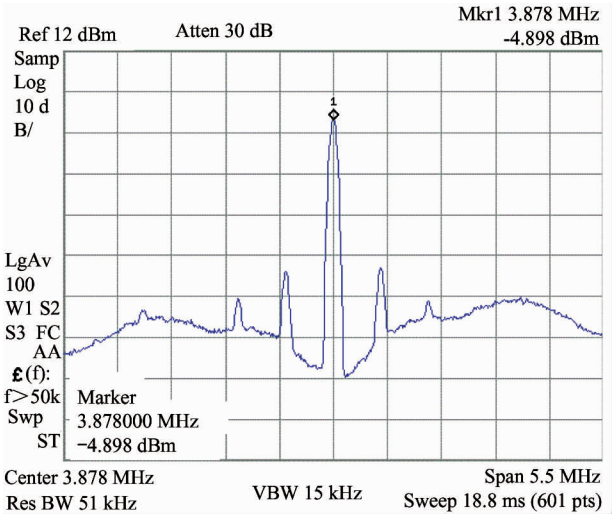



**Fig. 15** Output spectrum of the fractional frequency divider when the input frequency is 0.5 GHz and division ratio is 129.125

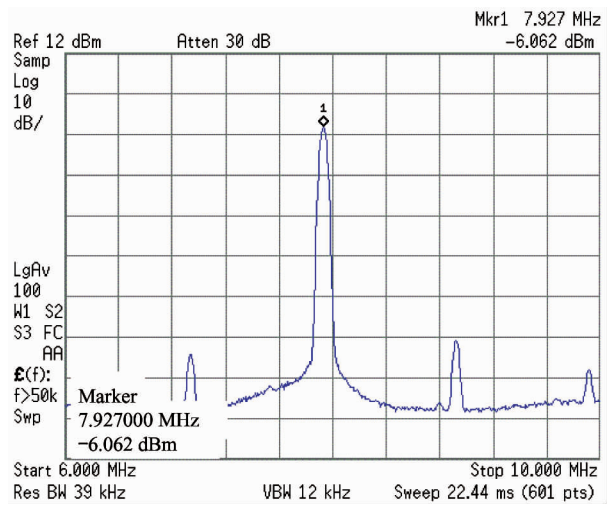



**Fig. 16** Output spectrum of the fractional frequency divider when the input frequency is 8GHz and division ratio is 1008.875

## 4 Conclusion

This paper presents a fractional frequency divider constituted by a high-speed divider-by-2, a 0.5 step programmable frequency divider based on phase switching, and a negative feedback delta-sigma modulator. The high-speed divider-by-2 is used to generate the

quadrature I/Q output signals for the transceivers. The phase-switching technique is adopted to obtain a 0.5 division step. And the negative feedback delta-sigma modulator is proposed to obtain the smooth output spectra for all the allowed inputs. The measured results show that the fractional frequency divider can work correctly with input frequency varying from 0.5 GHz to 8 GHz. With the 1.8 V supply voltage, when the input frequency is 8 GHz, the total current consumption of the whole divider is 17.5 mA, and the chip area is 0.58 $mm^2$, including the pads. However, since testing the output spectrum of the NF-DSM in the fractional frequency divider directly is difficult, its output spectrum is just measured through the FPGA. After finishing the whole frequency synthesizer, the output spectrum of the frequency synthesizer will be tested to validate the performance of the NF-DSM experimentally further.

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