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A new digital transmitter based on delta sigma modulator with bus-splitting①

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Abstract

A new digital transmitter based on delta sigma modulator (DSM) with bus-splitting is presented in this paper. The second order low pass error-feedback delta sigma modulator (EF-DSM) is focused. The signal to noise ratio (SNR) of the EF-DSM is derived for different bus-splitting bits. Following the EF-DSM, a multi-bit digital up mixer is used for carrier frequency transform. In order to validate the theory of bus-splitting, two types of transmitters are implemented on FPGA for comparison, in which one is with non-bus-splitting and the other is with bus-splitting. The FPGA implemented transmitter with bus-splitting promotes the maximum operation speed by 39%, and reduces hardware consumptions more than 16%. Both single tone and orthogonal frequency division multiplexing (OFDM) signal source are used to evaluate the proposed transmitter.

Key words: bus-splitting, error-feedback delta sigma modulator (EF-DSM), signal to noise ratio (SNR), digital transmitter, digital up mixer

0 Introduction

Modern wireless communication systems use high order modulation. Orthogonal frequency division multiplexing (OFDM) is used in many communication protocols for its high spectrum efficiency. However, OFDM signals are with non-constant envelop, and are of high peak average power ratio (PAPR). So, a linear power amplifier is required in the OFDM transmitter. For lower distortion of a linear power amplifier (PA), it often backs off severely. That leads to low drain efficiency of a power amplifier, and shortens working duration of battery supplied equipment. Many technologies have been developed to solve this contradiction. One of them is a transmitter based on delta sigma modulator (DSM) used in audio application for several decades. In late 1990s, it was proposed to be used in radio frequency (RF) power amplifier. The first application was targeted to RF signal centered at ten megahertz[1]. A band-pass DSM running at forty megahertz converted the RF signal into 2-level digital stream, and then a switch mode power amplifier was used instead of a linear one to boost the RF power. For the modern wireless communication system, signal bands are usually in several giga-hertz (GHz). The working frequency of the band-pass DSM calls for nearly ten gigahertz, which is challenge for implementation[2,3]. A low-pass DSM alleviates the requirement of processing speed because its working frequency is tens of the signal bandwidth. The outputs of the low-pass DSMs from the inphase (I) and quadrature (Q) branch are then multiplexed for up mixer conversion[3,4].

For adequate signal-to-noise ratio (SNR) in band, higher order or high oversampling ratio (OSR) DSMs are required. Single bit higher order DSM not only surfers from stability problems, but also the complexity that leads to challenging to promote the speed, which limits the maximum OSR. Special designed adders[3,5] should be designed for high speed operation. Another method for promoting the OSR is parallelized DSM or time-interleaved DSM (TI-DSM)[6,7]. Error-feedback DSM (EF-DSM) has a simple architecture, and is potential to run fast[8]. It is suitable for speed demanding DSM based transmitter applications. The multi-bit quantizer makes the EF-DSM stable. Compared with single bit DSM, the multi-bit DSM is with less quantizer noise, which also promotes the coding efficiency[2] of the transmitter. For the multi-bit quantizer used in EF-DSM, the transmitter needs multi-bit

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up conversion, which will be described in Section 3.

In this work, a new EF-DSM based transmitter with bus-splitting topology[9,10] is proposed to reduce the hardware complexity and increase the available clock speed of the EF-DSM, while providing adequate SNR. With introducing bus-splitting technique, the least-significant-bit part of the digital baseband signal is processed by a lower order EF-DSM, reducing hardware consumption. And with bus-splitting, the delay for the carry of the adders in EF-DSM is decreased, because the signal with large bit width is split into two signals with small bit width which are processed by individual adders. The clock speed of the EF-DSM with bus-splitting is promoted finally. The paper is organized as follows. Section 1 describes the general EF-DSM based transmitter structure. Section 2 derivates the SNR for the EF-DSM with bus-splitting topology. Simulation of a transmitter based on EF-DSM with bus-splitting is carried out in Section 3. In Section 4, the FPGA implemented transmitter is evaluated. Finally, conclusion is drawn.

1 General EF-DSM based transmitter structure

The block diagram of a general EF-DSM based transmitter is shown in Fig. 1, which is composed of four main parts[3-6]. The first part is an EF-DSM to convert the baseband multi-bit signal into signal with several bits by using multi-bit quantizer. There are two identical EF-DSMs to process the input quadrature I/Q components respectively. The second part is a digital frequency up-mixer which converts the signal into carrier frequency. The third part is a high efficient switch mode power amplifier (SMPA) boosting the RF power to drive the antenna and the last part is a band-pass filter removing the out-of-band quantization noise generated by the EF-DSM.

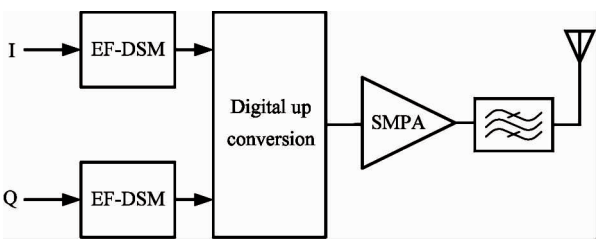


Fig. 1 Block diagram of a general EF-DSM based transmitter

The EF-DSM is shown in Fig. 2, the transfer function for an EF-DSM with order of L can be expressed in Eq. (1). It is the sum of two terms. One is the signal term, and it is related to the signal transfer function (STF). The other is the noise term, and it is related to noise transfer function (NTF).

$$Y(z) = STF(z)X(z) + NTF(z)E(z) \tag{1}$$

where $STF(z)$ is unit or delay, and $NTF(z)$ is usually a finite impulse response (FIR) filter. With different types of low-pass, band-stop or high-pass filter, the EF-DSMs are called high-pass (HP), band-pass (BP) or low-pass (LP) EF-DSMs respectively. With the NTF filter, the quantization noise was squeezed outside the signal band, which is called noise shaping. So, an EF-DSM can transform an original signal with multi-bit into a signal with merely several levels, and provide adequate SNR.

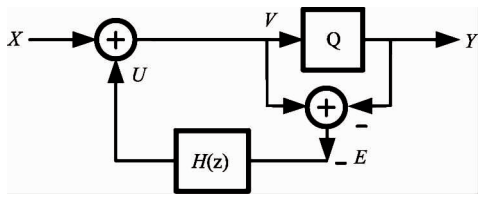


Fig. 2 Block diagram of the EF-DSM

An EF-DSM uses the quantization error as the feedback component. The quantizer of unsigned signal is simply realized by bus-splitting, which is a fast operation. The quantization error for the signed quantizer just needs additional inversion operation for the sign bit, which is still fast. The quantization error is then filtered by function $H(z)$, and is then added with the input. Function $H(z) = 1 - NTF(z)$ is also an FIR function, which is stable with several bits extension.

The derivation of SNR for EF-DSM is started as follows.

The in-band noise power with noise shaping is

$$N_{DSM}^2 = \frac{1}{12} \cdot \frac{\pi^{2L}}{(2L+1)OSR^{2L+1}} \tag{2}$$

For an N-bit input digital DSM, taking the quantization noise of the input signal into account, the following could be got:

$$N_0^2 = \frac{1}{12} \cdot \left(\frac{1}{2^{2N}OSR}\right) \tag{3}$$

The quantization noise in the output is

$$N^2 = \frac{1}{12} \cdot \left(\frac{\pi^{2L}}{(2L+1)OSR^{2L+1}} + \frac{1}{2^{2N}OSR}\right) \tag{4}$$

For any band-constrained signal with peak average power ratio (PAPR), the signal power can be revised as

$$P = \left(\frac{1}{2}\right)^2 \frac{1}{PAPR} \tag{5}$$

The SNR for any band-constrained signal with $PAPR$ is

$$SNR = \frac{P}{N^2} = \frac{3 \cdot 2^{2N}}{\frac{\pi^{2L}}{(2L+1)OSR^{2L+1}}2^{2N} + \frac{1}{OSR}} \cdot \frac{1}{PAPR} \tag{6}$$

According to Eq. (6), for a second order DSM with OSR of 16, a single tone signal input which can get SNR of 49dB, and SNR of 42dB for an OFDM signal with typical PAPR of 10 dB will be achieved. This study takes the second order EF-DSM as an example to conduct the following derivation of EF-DSM with bus-splitting.

2 EF-DSM with bus-splitting

The block diagram of the EF-DSM with bus-splitting topology is shown in Fig. 3. Two EF-DSMs, EF-DSM-M and EF-DSM-L for processing the split MSB and LSB part respectively, are used instead of the one EF-DSM used in the non-bus-splitting topology. In this paper, EF-DSM-M is second order and EF-DSM-L is first order. The input of the DSM for transmitter application is in two's complement binary format. With bus-splitting operation on a two's complement number x with N-bit resolution, another two's complement number x_{MSB} is got, which is the MSB part with M bits and an unsigned number x_{LSB}, which is the LSB part with N-M bits.

$$x = 2^{N-M}x_{MSB} + x_{LSB} \tag{7}$$

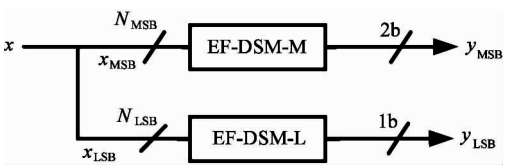


Fig. 3 Block diagram of EF-DSM with bus-splitting

In Z-domain, it can be calculated as

$$X = 2^{N-M}X_{MSB} + X_{LSB} \tag{8}$$

where X, X_{MSB} and X_{LSB} are the Z-transform of x, x_{MSB} and x_{LSB} respectively.

The MSB part is fed into EF-DSM-M, while the LSB part is treated as a signed number with an extending sign bit of zero, and is then fed into EF-DSM-L. EF-DSM-M outputs two-bit signed integer y_{MSB}, while EF-DSM-L outputs single bit signed integer y_{LSB}. The Z-domain expression for EF-DSM-M and EF-DSM-L can be written as

$$Y_{MSB} = X_{MSB} + (1 - z^{-1})^2 E_{MSB} \tag{9}$$

$$Y_{LSB} = X_{LSB} + (1 - z^{-1}) E_{LSB} \tag{10}$$

where E_{MSB} and E_{LSB} are the quantization noise for the two modulators.

The noise power for the output of EF-DSM-M and EF-DSM-L in signal band can be calculated as Eq. (11) and Eq. (12).

$$N_{MSB}^2 = \frac{1}{12}2^{2(M-N)}\frac{\pi^4}{5OSR^5} \tag{11}$$

$$N_{LSB}^2 = \frac{1}{12}2^{-2M}\frac{4\pi^2}{3OSR^3} \tag{12}$$

After the process, the two outputs are finally combined to get the final result.

$$y = 2^{N-M}y_{MSB} + y_{LSB} \tag{13}$$

In Z-domain, it can be written as

$$Y = 2^{N-M}Y_{MSB} + Y_{LSB} \tag{14}$$

Substituting Eq. (9) and Eq. (10) into Eq. (14), one gets:

$$Y = X + 2^{N-M}(1 - z^{-1})^2 E_{MSB} + (1 - z^{-1}) E_{LSB} \tag{15}$$

Considering the quantization noise in the original digital signal x, the total noise in the final result can be calculated as

$$N^2 = 2^{2(N-M)}N_{MSB}^2 + N_{LSB}^2 + N_0^2 \tag{16}$$

The final SNR of the bus-splitting DSM for signal with $PAPR$ input is in Eq. (17).

$$SNR = \begin{cases} \dfrac{3}{PAPR} \cdot \dfrac{2^{2N}}{\dfrac{1}{OSR} + \dfrac{\pi^2}{3OSR^3}2^{2N}}, & M = 0 \\ \dfrac{3}{PAPR} \cdot \dfrac{2^{2N}}{\dfrac{1}{OSR} + \dfrac{4\pi^2}{3OSR^3}2^{2(N-M)} + \dfrac{\pi^4}{5OSR^5}2^{2N}}, & 1 \leqslant M \leqslant N-1 \\ \dfrac{3}{PAPR} \cdot \dfrac{2^{2N}}{\dfrac{1}{OSR} + \dfrac{\pi^4}{5OSR^5}2^{2N}}, & M = N \end{cases} \tag{17}$$

For most baseband signals used in wireless transmitters, 12 – 14-bit resolution is adopted[3,4]. Fig. 4 plots SNR for a 13-bit input EF - DSM with different

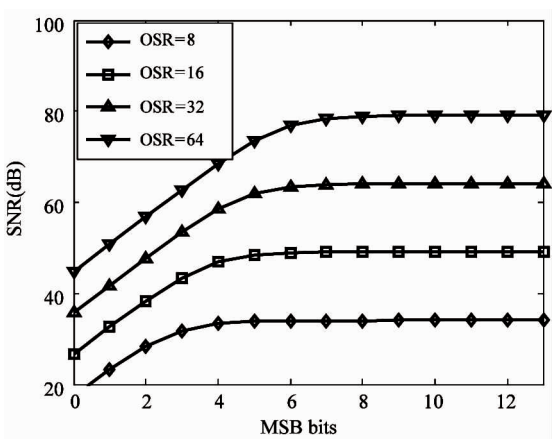


Fig. 4 SNR curve with different OSR for the 13-bit input bus-splitting EF-DSM versus different MSB bits

bus-splitting MSB bits for OSR from 8 to 64. When MSB bit number is larger than half of the total bits, with increasing MSB bits, the SNR increases only a little.

3 A new digital transmitter based on EF-DSM with bus-splitting

The architecture of the proposed transmitter based on EF-DSM with bus-splitting is shown in Fig. 5. The baseband (BB) signal is interpolated with 13-bit resolution. The quadrature I/Q components are fed into two EF-DSMs with the bus-splitting topology. The EF-DSM-M generates a two-bit stream, while the EF-DSM-L generates a one-bit stream. There are finally three-bit streams, so a three-bit digital up-converter is required to convert the signal into required carrier frequency. Then switch mode power amplifiers with proportional power as Eq. (13) are combined to get the required RF signal.

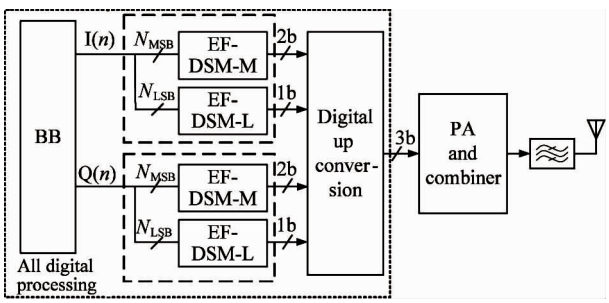


Fig. 5 Architecture for the proposed transmitter based on EF-DSM with bus-splitting

3.1 Digital up-converter

In a single bit transmitter, a multiplexer is used for up mixing the baseband signal into RF[3]. To implement the multiplexer based multi-bit mixer, a coding conversion unit is used before the up-conversion operation. For quantizer using mid-rise characteristic[11], the output from the DSM could be signed odd values like $\{\pm1, \pm3, \pm5\cdots\}$. The EF-DSM-M's output sequences coding in two-bit signed number are converted into two-bit symmetric binary number before bit-wise digital up conversion. In the symmetric binary number, bit '0' presents positive, while bit '1' presents negative. The symmetric binary number for the two-bit signed number of output of the EF-DSM-M $\{-3, -1, 1, 3\}$ can be converted as {11, 10, 01, 00}.

Fig. 6 shows the whole 3-bit up-conversion mixer for the transmitter. Taking the most significant bit (MSB) of the symmetric binary number for example, MSBs from both I and Q branches and their logic inverse values are multiplexed into a stream[3]. The intermediate significant bits (ISBs) and the least significant bits (LSBs) are processed with the same method.

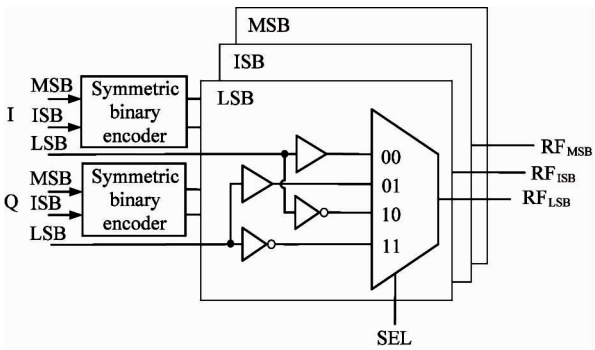


Fig. 6 The 3- bit digital up-conversion mixer

With the delay on the quadrature branch caused by the multiplexer, the phase balance is destroyed, leading image frequency in signal band and worsening the SNR. To compensate the delay, interpolation on the inphase branch should be done before it is processed by the DSM[12]. For fast computation, the linear interpolation is adopted. Because of the high oversampling rate, the accuracy of linear interpolation is enough[12]. Let f_s and f_c denote sampling frequency of the DSM and the carrier frequency respectively. Define the ratio of these two frequencies, $R = f_c/f_s$, the interpolation is done as

$$I'[n] = \frac{4R-1}{4R} I[n] + \frac{1}{4R} I[n-1] \tag{18}$$

3.2 Simulation results

The single tone signal and OFDM signal with QAM-64 are simulated respectively to evaluate the proposed transmitter based on EF-DSM with bus-splitting. Results are shown in Fig. 7 and Fig. 8. For single tone input, the non-bus-splitting structure achieves 48.8dB, in Fig. 7(a), and the bus-splitting structure with MSB part of 6 bits achieves 48.3dB, in Fig. 7(c). For OFDM input, the SNR for the two structures are 42.2dB (in Fig. 8(a)) and 41.3dB (in Fig. 8(c)) respectively.

The summarized SNR results for different MSB bits are plotted in Fig. 9. And the theoretical calculations are also plotted for comparison. Simulation confirms the theoretical calculation. From the figure, when the bit of MSB part decreases as low as four bits, SNR decreases only a little. It means that the hardware consumption can be reduced with decreasing MSB bits while remaining enough SNR.

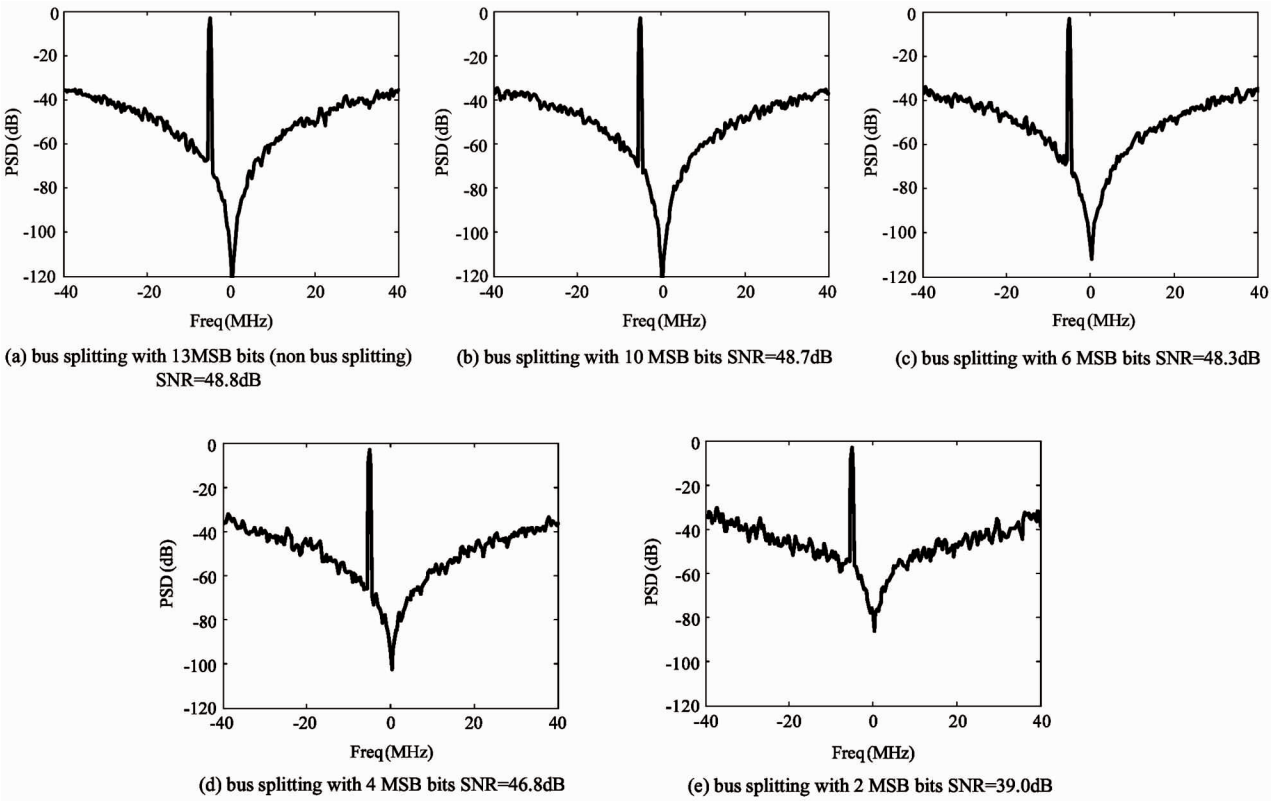


Fig. 7 Simulated spectrum of the transmitter with different bus-splitting combinations for single tone input

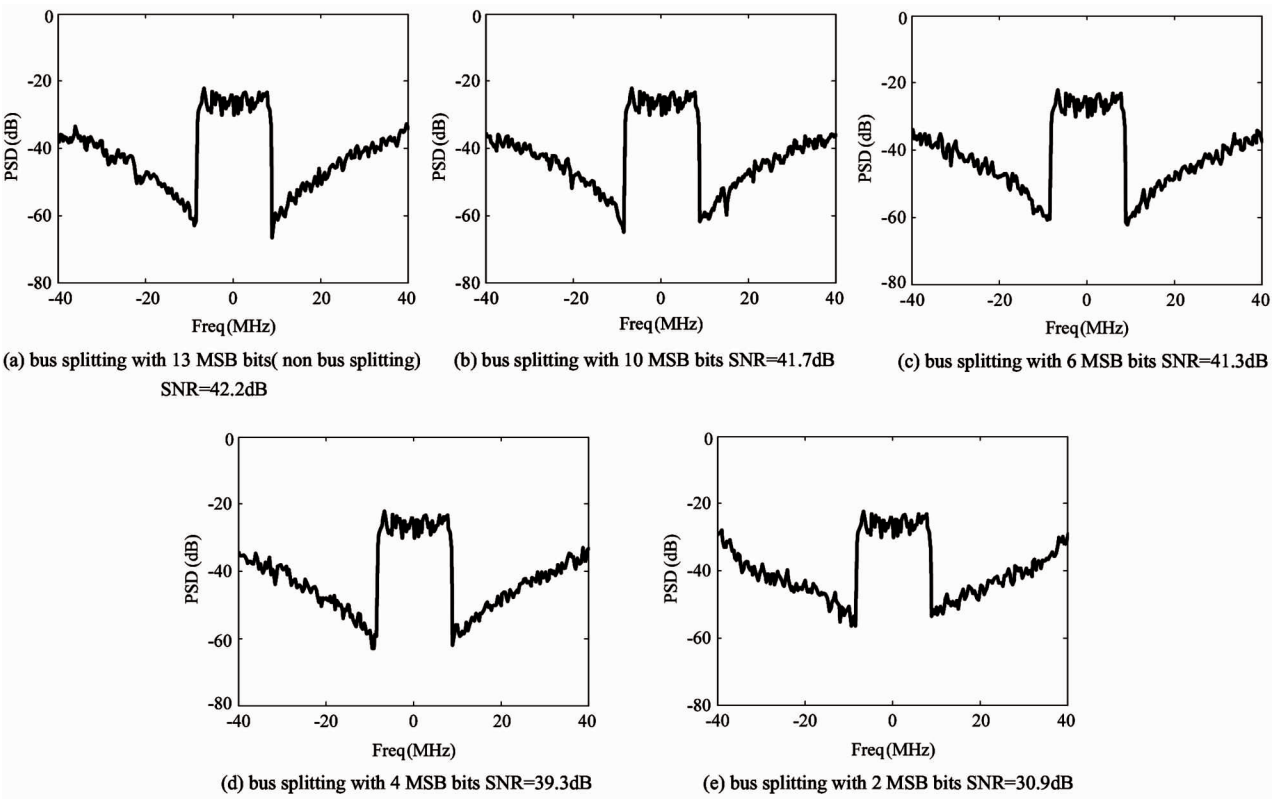


Fig. 8 Simulated spectrum of the transmitter with different bus-splitting combinations for 64-QAM OFDM signal input

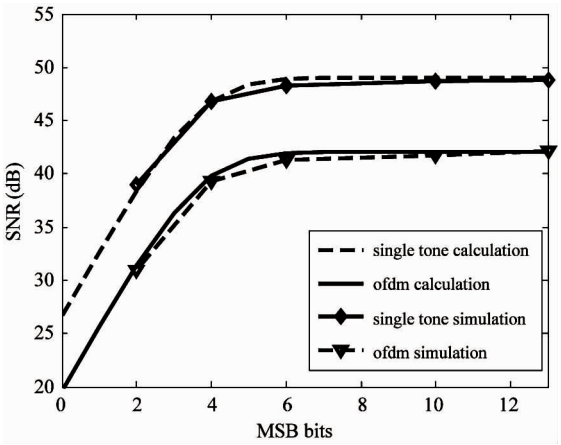
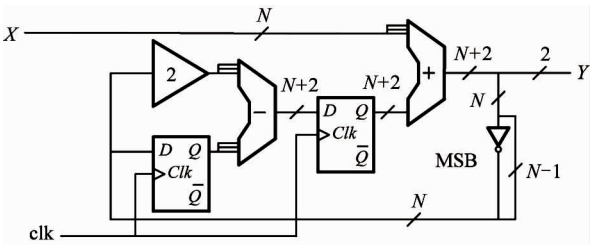


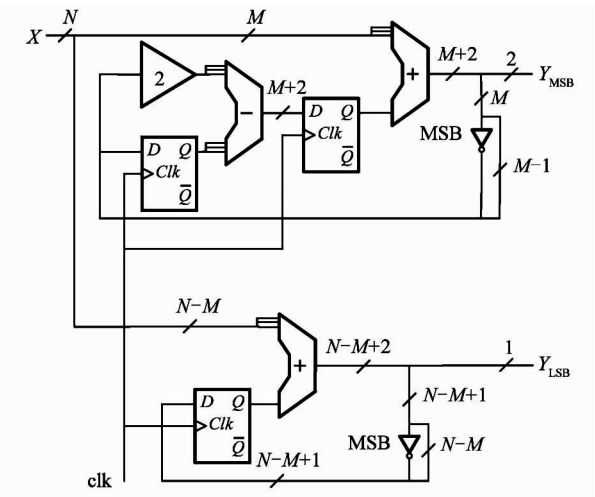
Fig. 9 SNR curve of single tone and OFDM signals for transmitter based on EF-DSM with bus-splitting

4 FPGA implementation and experiment result

The detailed register transfer level architecture for both EF-DSM with non-bus-splitting and bus-splitting is shown in Fig. 10. The EF-DSM with non-bus-splitting is implemented as Fig. 10(a), while the 13-bit data is fed into a single EF-DSM, as one input of the adder. The two most significant bits of the adder's output are split as the output of the DSM. The left thirteen least significant bits are treated as the errors of the quantizer, and then are filtered by a filter, finally are fed into the first adder as another input. The coefficient 2 in the filter is realized by left shifting. The EF-DSM with bus-splitting is shown in Fig. 10(b). The 13-bit data is first split into two parts. The MSB part is processed by a second order EF-DSM, and two bits are output. The split LSB part is fed into another first order EF-DSM. The most significant bit of the adder's output is split as the output. The left least significant bits are treated as the quantization error, then delayed and fed back into the first adder as another input. The EF-DSM with non-bus-splitting and bus-splitting are of two and three bits output respectively. Both the EF-DSM with non-bus-splitting and EF-DSM with bus-splitting of different MSB bits are implemented on FPGA.



(a) Second order EF-DSM without bus-splitting



(b) EF-DSM with bus-splitting

Fig. 10 Non-bus-splitting and bus-splitting EF-DSMs implemented in FPGA

4.1 Synthesized results of the EF-DSM

The hardware consumption with different bus-splitting bits is plotted in Fig. 11. The curve is monotonous. However, the curve for maximum clock speed in Fig. 12 is not monotonous . The speed limitation is

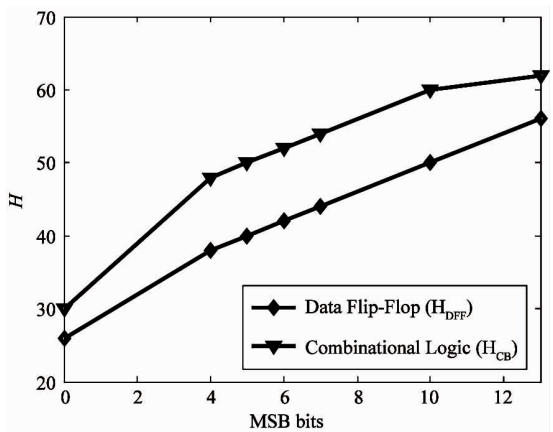


Fig. 11 Hardware consumption versus different bus-splitting bits

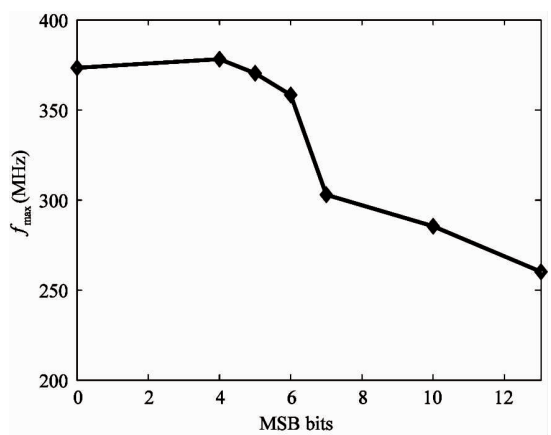


Fig. 12 Available maximum speed for different bus-splitting bits

caused by the carry out delay in adders. The larger the word length is, the more the delay increases. So, the clock speed for non-bus-splitting DSM is lower than the bus-splitting one.

The figure of merit (FOM) is taken as expressed in Eq. (19) to evaluate the bus-splitting EF-DSM. FOM reflects the tradeoff of speed, SNR and hardware consumption.

$$FOM = \frac{f_{\max} \cdot SNR}{H_{\mathrm{DFF}} H_{\mathrm{CB}}} \tag{19}$$

where $f_{\max}$ is the maximum clock speed of the EF-DSM, H_{DFF} and H_{CB} are hardware consumption of data flip-flops and combinational logic respectively.

FOM with different bus-splitting bit is plotted in Fig. 13. It can be seen that when the 13-bit bus is split with MSB part of 6 bits, the FOM gets the highest. Table 1 shows the hardware consumption and maximum clock speed of non-bus-splitting EF-DSM ($M = 13$) and bus-splitting with MSB part of 6 bits. The hardware consumption is reduced by more than 16% and the clock speed is promoted by 39% for the bus-splitting topology, and the resulted clock speed of 358MHz fulfills the sampling speed of oversampling rate of 16 for a signal with 20MHz bandwidth, which is 320MHz, while the non-bus-splitting topology cannot achieve the required 320MHz.

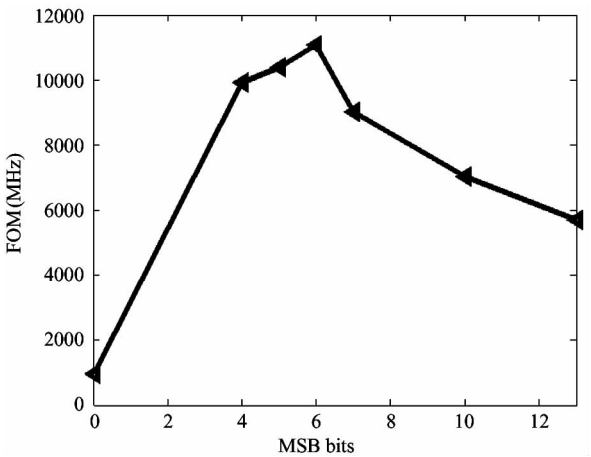


Fig. 13 FOM for different bus-splitting bits

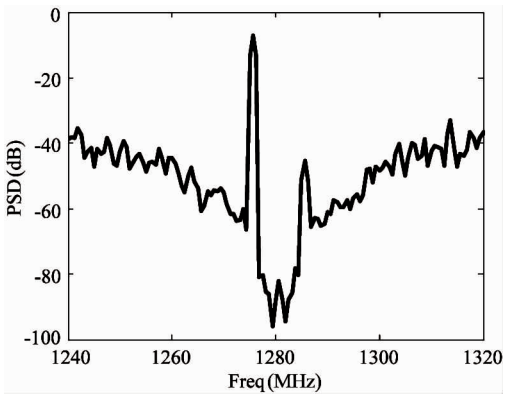
Table 1 Comparison of synthesized results for non-bus-splitting and bus-splitting EF-DSM

MSB part M bits	Data flip-flops	Combinational functions	$f_{\max}$ (MHz)
13	56	62	257
6	42	52	358
Percentage M6/M13	75%	84%	139%

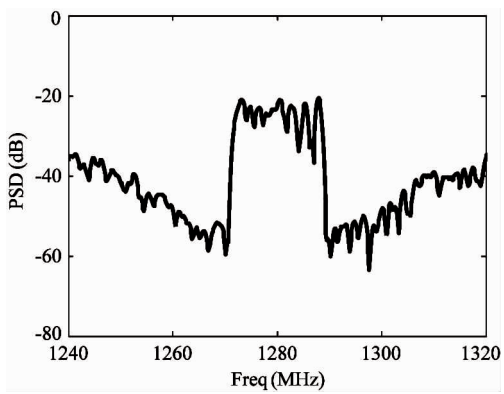
4.2 Experiment results

The proposed transmitter based on EF-DSM with bus-splitting is tested in FPGA. The single tone and the IEEE 802.11g compiled 64-QAM OFDM baseband signal with 16-times interpolation are first generated using Matlab. Then, they are stored in FPGA as the stimulus to the designed transmitter. The IQ baseband signals are fed into the FPGA implemented EF-DSMs with bus-splitting, the output streams are then fed into the FPGA implemented multiplexer based multi-bit digital up conversion stage, 1.28GHz is selected as the carrier frequency. The processed three-bit streams are stored and feedback to PC.

The output spectra for the transmitters based on EF-DSM with bus-splitting are calculated according to the processed bit streams, which are shown in Fig. 14. The single tone SNR shown in Fig. 14(a) is 45dB, and the OFDM SNR shown in Fig. 14(b) is 39dB.



(a) single tone input with bus-splitting, SNR = 45dB



(b) 64-QAM OFDM input with bus-splitting, SNR = 39dB

Fig. 14 spectra of the transmitter

5 Conclusion

This paper proposes a new transmitter based on EF-DSM with bus-splitting. The SNRs of EF-DSM with different numbers of bus-splitting bits are given by derivation. Simulation is conducted to validate the theoret-

ical analysis. The transmitters based on EF-DSM with bus-splitting of 6-bit MSB part and non-bus-splitting are implemented on FPGA. With bus-splitting, the hardware consumption was reduced to 84%, while the available maximum speed was 358MHz. The SNR of 64-QAM OFDM signal is 39dB, which fulfills the signal quality for IEEE 802.11g. It is valuable for the bus-splitting structure; however, the multi-bit transmitter may suffer from bit mismatch errors. This problem will be discussed in the future work.

References

[1] Jayaraman A, Chen P F, Hanington G, et al. Linear high-efficiency microwave power amplifiers using bandpass delta-sigma modulators [J]. *IEEE Microwave Guided Wave Letter*, 1998, 8(3): 121-123

[2] Johnson T, Stapleton S P. RF. Class-D amplification with bandpass sigma-delta modulator drive signals[J]. *IEEE Transactions on Circuits and Systems—I: Regular Papers*, 2006, 53(12): 2507-2520

[3] Frappé A, Flament A, Stefanelli B, et al. An all-digital RF signal generator using high-speed DS modulators[J]. *IEEE Journal of Solid-State Circuits*, 2009, 44(10): 2722-2732

[4] Silva N V, Oliveira A S R, Gustavsson U, et al. A novel all-Digital multichannel multimode RF transmitter using delta-sigma modulation[J]. *IEEE Microwave and Components Letters*, 2012, 22(3): 156-158

[5] Jerng A, Sodini C G. A wideband $\Delta\Sigma$ digital-RF modulator for high data rate transmitters[J]. *IEEE Journal of Solid-State Circuits*. 2007, 42(8):1710-1722

[6] Cordeiro R F, Oliveira A S R, Vieira J, et al. Wideband all-digital transmitter based on multicore DSM[C]. In: Proceedings of the 2016 IEEE MTT-S International Microwave Symposium (IMS), San Francisco, USA, 2016. 1-4

[7] Majd N E, Ghafoorifard H, Mohammadi A. Bandwidth enhancement in delta sigma modulator transmitter using low complexity time-interleaved parallel delta sigma modulator[J]. *AEü-International Journal of Electronics and Communications*. 2015,69(7): 1032-1038

[8] Afzal N, Wikner J J, Gustafsson O. Reducing complexity and power of digital multibit error-feedback delta sigma modulators[J]. *IEEE Transactions on Circuits and Systems-II Express Briefs*, 2014, 61(9): 641-645

[9] Fitzgibbon B, Kennedy M P, Maloberti F. Hardware reduction in digital delta-sigma modulators via bus-splitting and error masking—part II: non-constant input [J]. *IEEE Transactions on circuits and systems-I: regular papers*. 2012,59(9): 1980-1991

[10] Fitzgibbon B, Kennedy M P, Maloberti F. Hardware reduction in digital delta-sigma modulators via bus-splitting and error masking—part I: constant input [J]. *IEEE Transactions on circuits and systems-I: regular papers*, 2011, 58(9):2137-2148

[11] R Schreier. Understanding Delta-Sigma Data Converters [M]. Wiley, 2005

[12] Frappé A, Flament A, Stefanelli B, et al. All-digital RF signal generation for software defined radio[C]. In: Proceedings of the 4th European Conference on Circuits and Systems for Communications, Bucharest, Romania, 2008. 236-239

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